A Three-Phase Version of the Hybridge Rectifier Associated to the Three-Phase ZVS DC/DC Converter with Asymmetrical Duty Cycle

Demercil S. Oliveira Jr.[1], Student Member, IEEE, Ivo Barbi[2], Senior Member, IEEE

[1] INEP, UFSC, Florianópolis, Brazil, e-mail : demercil@inep.ufsc.br
[2] INEP, UFSC, Florianópolis, Brazil, e-mail : ivobarbi@inep.ufsc.br

***Abstract*— This paper proposes the use of a three-phase version of the hybridge rectifier in the three-phase ZVS dc/dc converter with asymmetrical duty cycle. The use of this new rectifier improves significantly the efficiency of the converter because only three diodes are responsible for the conduction losses in the secondary side. Besides, the current in the secondary side of the transformer is half of the output current. In addition, all the advantages obtained in the three phase dc/dc converter, i.e. the increase of the frequency of the output and input currents, the improved distribution of the losses as well as the soft commutation for a wide load range, are preserved. Then, the resulting topology is viable to achieve high efficiency and high power density at high power levels. The theoretical analysis, simulation and experimental results obtained with a prototype of 6kW, as well as the comparison of the efficiency with the full bridge rectifier are presented.**

***Index Terms*— three phase dc/dc converter, asymmetrical duty cycle, hybridge rectifier.**

I. INTRODUCTION

Nowadays, the main topology used in high power dc/dc conversion is the ZVS PWM Full Bridge converter [1][2]. It is characterized by four switches operating in high frequency. The soft commutation can be obtained by using phase shift modulation, which preserves the simplicity and achieves high power density.

However, for higher power levels, the components face several stresses. As possible solutions, the parallelism of components or even converters can be applied. The former choice increases the complexity of the compromise between the layout circuit and the thermal design. Besides that, one should consider that the dynamic and static current sharing problem limits its application. The other alternative causes redundancy in the control circuits as well as in the number of power components and drivers, increasing the global cost and size of the equipment.

A prominent alternative was proposed by Ziogas [3]. It uses a three-phase inverter coupled to a three-phase high frequency transformer and to a three-phase high frequency rectifier. The resulting advantages consist in the increase of the input and output current frequency, by a factor of three compared to the Full Bridge converter, lower rms current through power components and reduction of the cores.

Although it presents satisfactory advantages, soft commutation has not been achieved, which limits the switching frequency and the power density. Then, the use of the asymmetrical duty cycle [4] in the three-phase dc/dc converter was proposed [5], in order to provide the ZVS commutation of all switches for a wide load range. Nevertheless, the resulting topology suffers high conduction losses, since two series diodes conduct the load current.

II. THE PROPOSED THREE PHASE HYBRIDGE RECTIFIER

In order to overcome the efficiency limit imposed by the full bridge rectifier used in [5], the extension of the hybridge converter [6] for its three-phase version is proposed, as shown in Fig. 1. This rectifier is formed by only three diodes and three inductors, but provides the same optimum transformer utilization as the four diode Full-Bridge rectifier. Additionally, current through secondary winding is a half of the output current. On the other hand, although the inductors size is theoretically maintained, the three separate inductors will actually occupy a greater volume. In order to avoid this penalty, these inductors can be combined into a three-phase core. Since the waveforms obtained with such inductor configuration are different, the study of this alternative will consist in the scope of subsequent works.

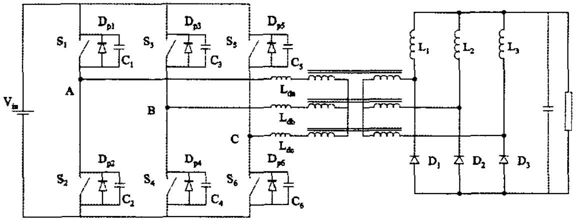

Fig1. - Three-phase ZVS dc/dc converter with the hybridge rectifier.

III. OPERATING MODES

The study of the waveforms relevant to the proposed converter reveals the existence of several operating modes, depending on the duty cycle and output current. Each operating mode has distinct sequences of stages and they will be named as DMIN, DMED and DMAX.

A. Stages in DMIN operation mode (Fig. 5)

First stage (Fig. 2): the switch S_6 turning off causes the linear transition of all line currents. The rectifier diodes D_1, D_2 and D_3 conduct and the currents in the output inductors decrease linearly.

Second stage (Fig. 3): at the moment when current i_{Ldc} reaches i_{L3}, the diode D_3 is blocked and energy is transferred to the load.

Third stage (Fig. 4): the switch S_5 turning off ceases the energy transference and causes a freewheeling stage to begin, in which all currents and voltages remain constant, until switch S_2 turns off. Then, the same behavior is assumed for the remaining switches.

0-7803-7912-8/03/$17.00 © 2003 IEEE

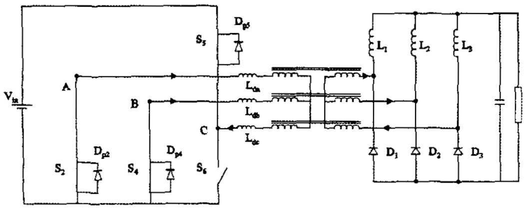

Fig. 2 – First stage in mode DMIN.

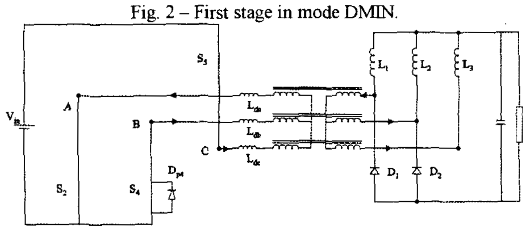

Fig. 3 – Second stage in mode DMIN.

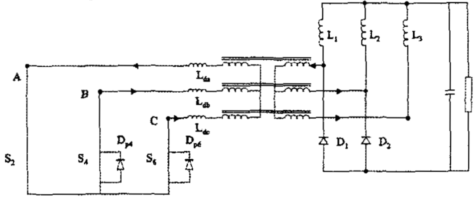

Fig. 4 – Third stage in mode DMIN.

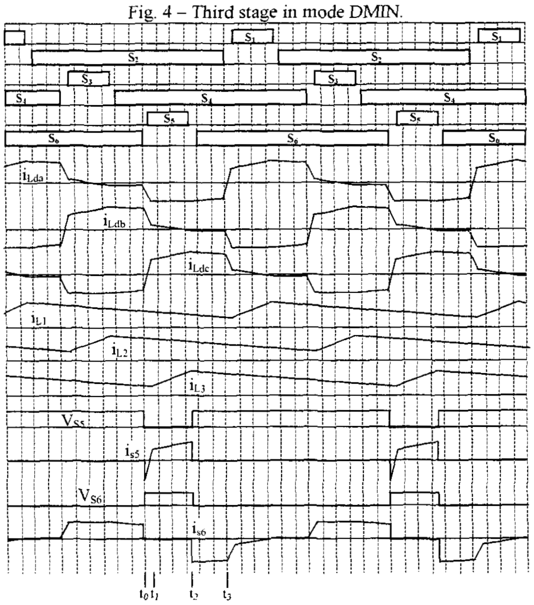

Fig. 5 – Main waveforms in mode DMIN.

B. Stages in DMED operation mode (Fig. 9)

First stage (Fig. 6): the switch S_6 turning off causes the linear transition of the line currents in phases *a* and *c*. The rectifier diodes D_1 and D_3 conduct and nearly a half of the input voltage is transferred to the load.

Second stage (Fig. 7): at the moment that current i_{Ldc} reaches i_{L3} the diode D_3 is blocked and energy is transferred to the load.

Third stage (Fig. 8): the switch S_3 turning off causes D_2 to be forward biased, but energy continues to be transferred to the secondary until the switch S_2 turning off. Then, the same behavior is assumed for the remaining switches.

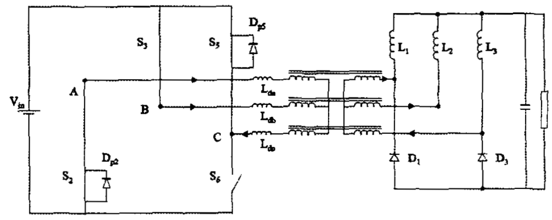

Fig. 6 – First stage in mode DMED.

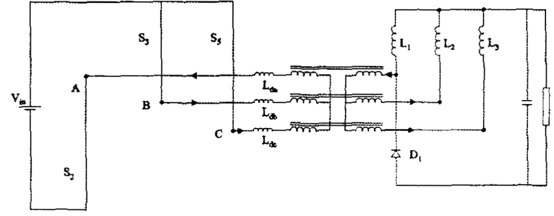

Fig. 7 – Second stage in mode DMED.

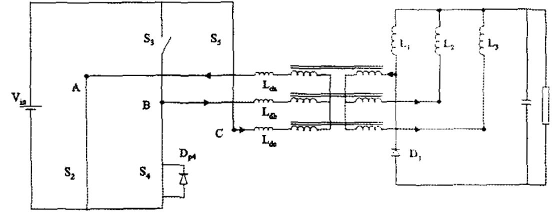

Fig. 8 – Third stage in mode DMED.

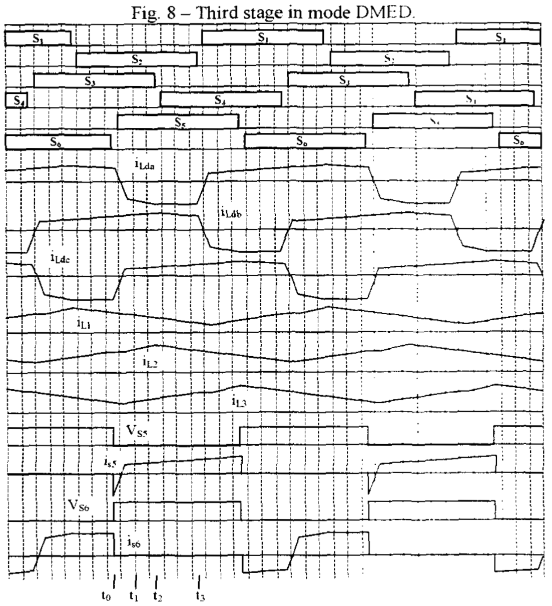

Fig. 9 – Main waveforms in mode DMED

C. Stages in DMAX operation mode (Fig. 13)

First stage (Fig. 10): the switch S_6 turning off causes all rectifier diodes to be forward biased. Then, no energy is transferred to the load and the currents decrease according to the output voltage.

Second stage (Fig. 11): at the moment that S_1 turns off, a linear transition between the line currents *a* and *c* begins. Besides a half of the input voltage is transferred to the load.

Third stage (Fig. 12): when the line current in phase *c* reaches i_{L3}, diode D_3 is blocked and an energy transference stage begins.

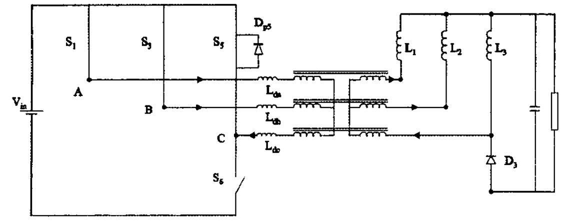

Fig. 10 – First stage in mode DMAX.

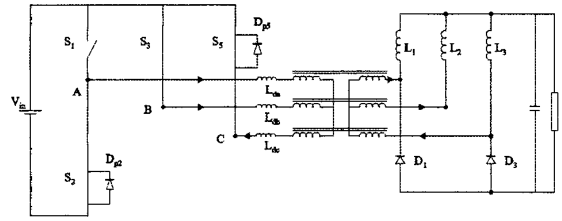

Fig. 11 – Second stage in mode DMAX.

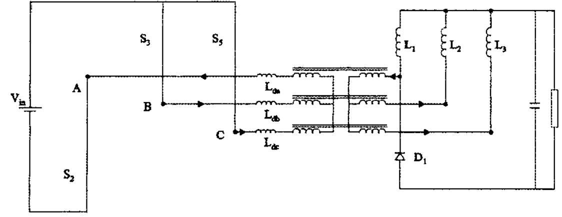

Fig. 12 – Third stage in mode DMAX.

According to the previously presented operation modes, the time intervals and voltages on the output filters, corresponding to each topological state can be obtained, as shown in Table 1. For simplicity, the parameterized current I_0' and inductance factor k are defined as:

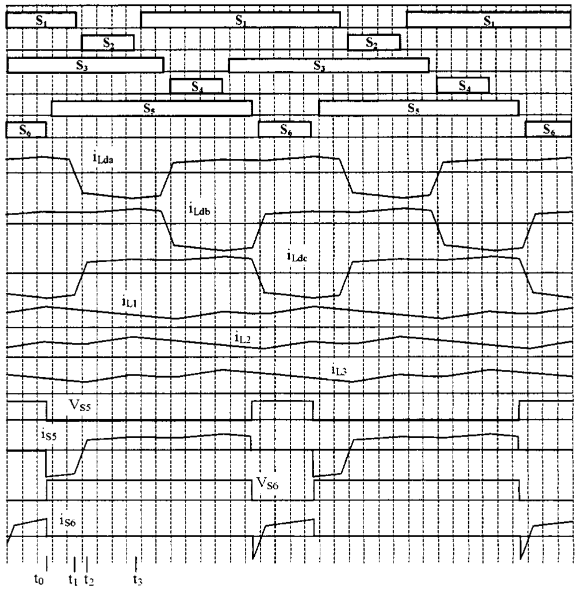

Fig. 13 – Main waveforms in mode DMAX.

$$I_0' = \frac{f_s L_d I_0}{V_{in}} \tag{1}$$

$$k = \frac{L_d}{L_f} \tag{2}$$

where $L_d=L_{da}=L_{db}=L_{dc}$ are the transformer leakage inductances, $L_f=L_1=L_2=L_3$ is output filter inductance, V_{in} is the input voltage and T_s corresponds to the switching period, as all the parameters are referred to the secondary side of the transformer.

Table 1
Voltages on the output inductors and time intervals.

	DMIN			DMED			DMAX		
	STAGE 1	STAGE 2	STAGE 3	STAGE 1	STAGE 2	STAGE 3	STAGE 1	STAGE 2	STAGE 3
V_{L1}	0	0	0	0	0	0	0	0	0
V_{L2}	0	0	0	$\frac{(V_{in}-V_0)}{3k+2}$	$\frac{(V_{in}-V_0)}{3k+1}$	0	0	$\frac{(V_{in}-2V_0)}{3k+2}$	$\frac{(V_{in}-V_0)}{3k+1}$
V_{L3}	0	$\frac{(V_{in}-V_0)}{1,5k+1}$	0	0	$\frac{(V_{in}-V_0)}{3k+1}$	$\frac{(V_{in}-V_0)}{k+1}$	0	0	$\frac{(V_{in}-V_0)}{3k+1}$
Δt	I_0'	DT_s-I_0'	$T_s\left(\frac{1}{3}-D\right)$	$2I_0'$	$T_s\left(D-\frac{1}{3}\right)-2I_0'$	$T_s\left(\frac{2}{3}-D\right)$	$T_s\left(D-\frac{2}{3}\right)$	$2I_0'$	$T_s(1-D)-2I_0'$

IV. OUTPUT CHARACTERISTIC AND SOFT COMMUTATION CONDITION

From the theoretical analysis shown in Table 1, one can state the conditions for each operating mode as well as the respective output characteristic, as shown in Table 2. One can see that the equations describing each operating mode do not include an interval between DMIN and DMED. In this interval, named DINT, a linear transition stage is interrupted by the turning off of one switch, as another linear transition stage with different derivative begins. Its output characteristic is considered constant and given by:

$$G = \frac{1}{3} - I_0' \tag{3}$$

Then, the graph of the output characteristic versus duty cycle can be plotted, as shown in Fig. 14. In addition, Table 2 shows the load condition for soft commutation, where $Z_0 = \sqrt{L_d/C}$. The constant value in the numerator is present because the currents in the output inductors are one third of the output current. Besides, the constant value in the denominator represents the leakage association in each operating mode. In the modes in which there is no minimum load condition to get ZVS commutation, the output inductors are connected in series with the switches.

Table 2
Operation modes conditions and output characteristic.

	DMIN	DMED	DMAX
Conditions	$D > I'_0 \wedge D \leq \frac{1}{3}$	$D > \frac{1}{3} + 2I'_0 \wedge D \leq \frac{2}{3}$	$D > \frac{2}{3} \wedge D \leq 1 - I'_0$
Output Characteristic	$G = D - I'_0$	$G = D - 3I'_0$	$G = 2 - 2D - 3I'_0$
Load condition for soft commutation of switches S_2, S_4 e S_6	0	0	$I'_0 > \frac{3}{\sqrt{2}} \frac{V_{in}}{Z_0}$
Load condition for soft commutation of switches S_1, S_3 e S_5	$I'_0 > \frac{3}{\sqrt{1.5}} \frac{V_{in}}{Z_0}$	$I'_0 > \frac{1.5}{\sqrt{2}} \frac{V_{in}}{Z_0}$	0

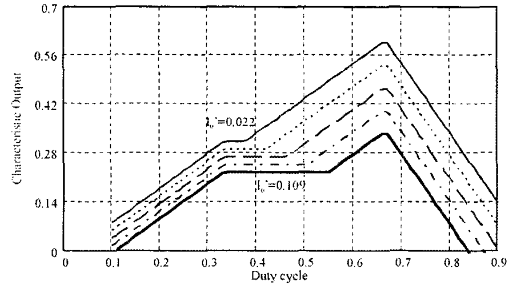

Fig. 14 – Output Characteristic.

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, simulation results concerning this topology, with the parameters set shown in Table 3, are presented in Fig. 15.

As it can be noticed in Fig. 12, the waveforms are typically referent to the mode DMED. The line currents i_{Lda}, i_{Ldb} and i_{Ldc} are unbalanced, what suggests a special adjustment in the practical implementation of the output inductors. The remaining waveforms validate the theoretical analysis.

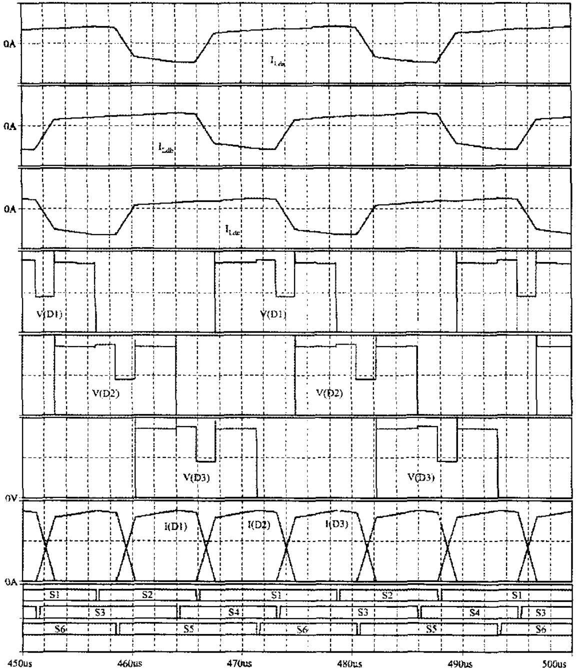

Fig. 15 – Main waveforms of the circuit in mode DMED obtained via simulation.

Table 3
Simulation parameters set.

V_{IN}	N	P_0	L_D	L_F	D	T_S	I_0
420 V	2.25	6kW	10μH	45μH	0.582	21.9μs	85A

In order to obtain the experimental results, a prototype with the same parameters set used in simulation has been built. The following results were obtained with the converter operating in the maximum output voltage mode. Fig 16 shows current and voltage in switch S_5, in which ZVS commutation can be visualized. In addition, Fig. 17 presents the obtained waveforms in switch S_6, where, one can see that all switches commutate in ZVS mode.

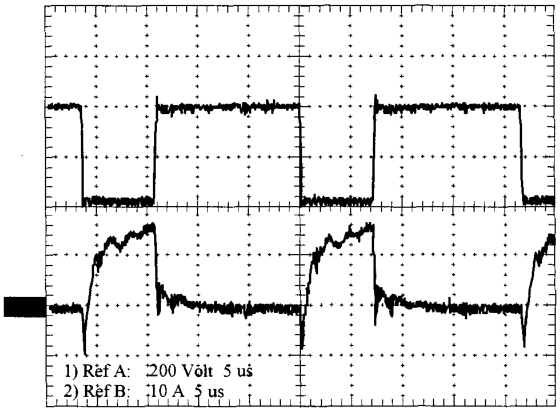

Fig. 16 – Voltage and current in switch S_6.

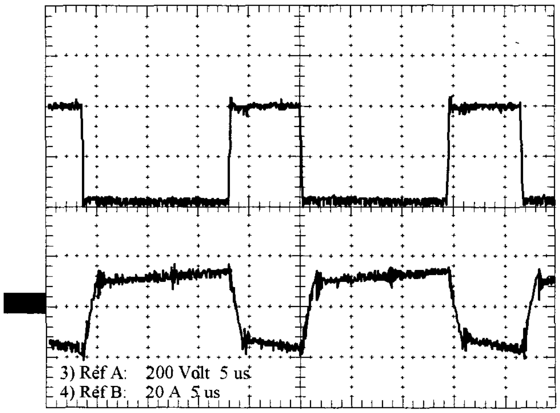

Fig. 17 – Voltage on switch S_5 and current in L_{dc}.

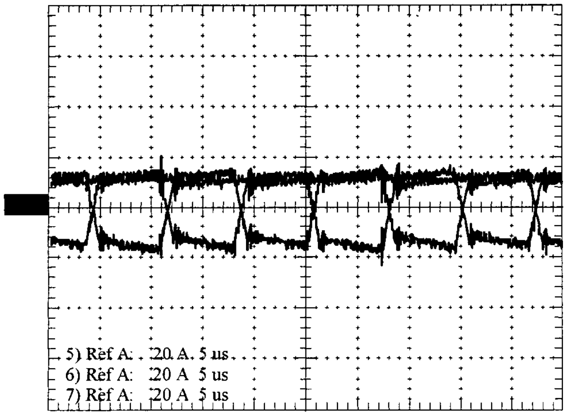

Fig. 18 – Line currents i_{Lda}, i_{Ldb} and i_{Ldc}.

Fig. 18 shows the obtained line currents i_{Lda}, i_{Ldb} and i_{Ldc}. The waveforms demonstrate satisfactory equilibrium among the line currents. In Fig 19, one can see the currents in output inductors L_1, L_2 and L_3. A difference equal to 15% of the output current between the currents i_{L1} and i_{L3} was measured but considered acceptable.

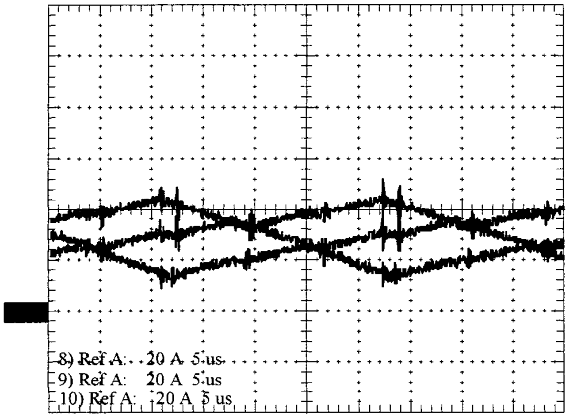

Fig. 19 – Voltage and current in switch S_6.

Fig. 20 shows that the use of a three-phase version of the Hybridge rectifier improves substantially (about 2%) the efficiency of the three-phase ZVS dc dc converter with asymmetrical duty cycle when compared to the three-phase Full-Bridge rectifier.

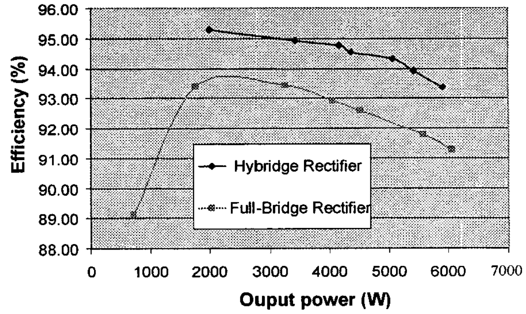

Fig. 20 – Efficiency obtained with the Hybridge rectifier and with the Full-Bridge rectifier.

VI. CONCLUSIONS

This paper has presented the use of a three-phase version of the hybridge rectifier, in the three-phase dc dc converter with asymmetrical duty cycle. This approach has improved substantially the global efficiency of the converter (about 2%) since only one diode conducts the load current.

In the Hybridge configuration, the output filter volume is theoretically maintained and only three rectifier diodes are used. In addition, the sink requirements for theses semiconductors are smaller, since that losses are dramatically reduced in the secondary side.

The theoretical waveforms as well as the output characteristic and the soft commutation conditions have been analyzed for all operational modes. Furthermore, a prototype of 6kW of the proposed converter has been developed in laboratory and the relevant results are presented.

VII. REFERENCES

[1] I. Barbi, W.A. Filho, "A Non-Resonant Zero Voltage Switching Pulse Width Modulated Full-Bridge DC/DC Converter," in Proc. IECON 1990, pp 1051-1056.

[2] R.L. Steingerwald, K.D.T. Ngo, "Full-Bridge Lossless Switching Converter," U.S. Patent 4864479, Sept 5, 1989

[3] P.D. Ziogas, A.R. Prasad, S. Manias, "Analysis and design of a three phase off-line dc-dc converter with high frequency isolation," IN Proc IAS 88, pp. 813 – 820

[4] N. Mohan, P. Imbertson, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," IEEE Transactions on Industry Applications, vol 29 no 1, jan/feb 1993, pp 121-125

[5] D.S. Oliveira Jr, I. Barbi, "A dc/dc ZVS three phase converter with asymmetrical duty cycle," under submission in IEEE Transactions on Power Electronics.

[6] C. Peng, M. Manningan, O. Seiresen, "A new efficient high frequency rectifier circuit," Proceding of HFPC 1991, Toronto, Canada, pp. 282-292, June 9-14, 1991.