

A Three Level Double-Ended Flyback Converter

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Abstract— A new four-switch converter topology is presented. This topology is intended for use in high input voltages and low power applications, especially auxiliary supplies. Its main advantage is the clamping voltage on the switches: half of the input voltage. It works like the flyback converter, with one direction power flow. The four switches can be set on with the same pulse, with a small delay time in the off signal of the internal switches after the external ones. The reliability of the converter is increased with the series position of the switches with the load. This reliability combined with the simplicity of the way it is commanded, makes this converter very well suited for small power applications. This paper presents the principle of operation of the proposed converter. Each stage with the main characteristics, and the main equations are also presented. Experimental data prove the suitability of the proposed converter.

Index Terms—DC-DC converters, high input voltage converter, auxiliary supplies.

I. INTRODUCTION

In telecommunication energy systems, or motor drive applications, the power supply is commonly composed by a power factor correction rectifier (ac-dc converter) [4, 5]. To achieve power factor correction (PFC), the topology generally used is the boost rectifier, which presents an output voltage greater than the peak of the AC input voltage. These kinds of converters enclose, usually, auxiliary supplies connected at the DC link. These auxiliary sources must start up before anything in the power supply system. Even when the main power system fails,

sometimes is very interesting that the auxiliary supply continue to works, to permit that remote communication circuits or any electronic supervision could stay in stand by, and transmit information about the fail, for example.

Most of the popular topologies used in auxiliary supplies present as a drawback the off-voltage stress over the main switch [2, 3, 7, 8, 9]. This voltage is twice the input voltage of the converter (e.g. flyback, forward). As one answer to the investigation on reliable converters, which also reduce the off-voltage stress on the switches, and could be implemented with relative simplicity, the three level double-ended flyback converter [1] is stated.

II. THE DC-DC THREE LEVEL DOUBLE-ENDED FLYBACK CONVERTER

A. Circuit Description

The three level flyback converter proposed in this paper is shown in Fig. 1. The four switches are indicated by the S_1 , S_2 , S_3 and S_4 MOSFETs. The input capacitors with the voltages V_{C1} and V_{C2} split the input voltage E . The clamping diodes D_{C1} and D_{C2} certify the voltage on the switches S_1 and S_4 to be half of the input voltage. The D_1 and D_2 diodes permit the energy stored in the leakage inductance to be dissipated on the input supply.

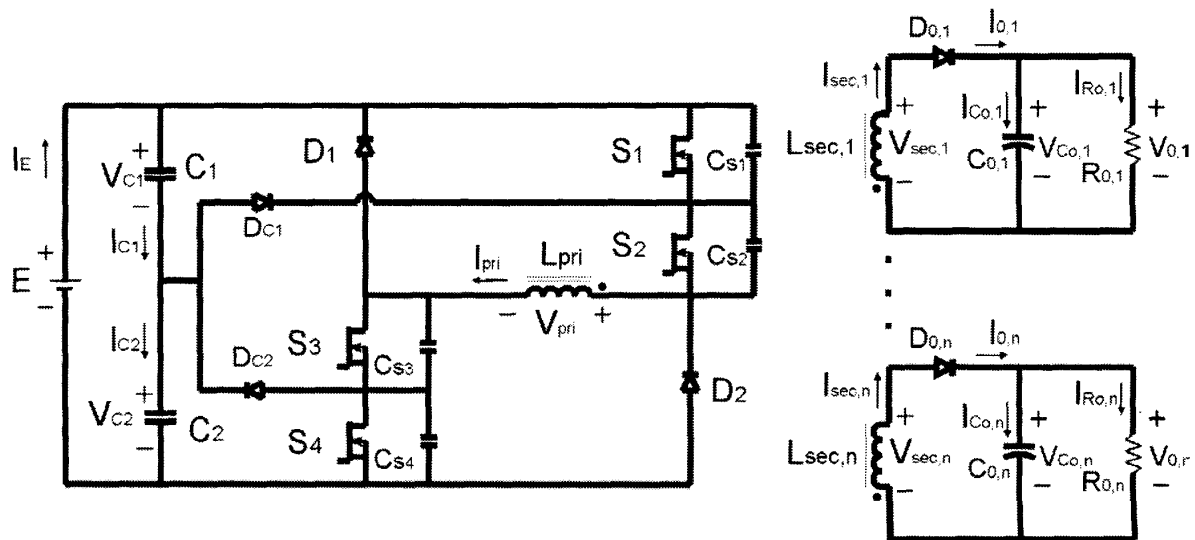


Fig. 1 – Three Level Flyback Converter.

The output stage is composed by the rectifier diode D_O and the load represented by the capacitor C_O and the resistor R_O . As an application for low power converter, this one could work with several outputs. This possibility is also showed in Fig. 1, with the index number on the secondary side elements representing n -outputs.

B. Operations stages

To simplify the analysis some suppositions are made: 1) the circuit operates in steady state; 2) all power semi-conductors are ideal; 3) the intrinsic capacitances of the MOSFETs are equal and constants, and are indicated by C_{S1} , C_{S2} , C_{S3} and C_{S4} .

The six stages of operation are presented in Fig. 2. The main waveforms that correspond for each stage can be observed in Fig. 3. The operation is described as follows:

First stage (t_0, t_1): This is the stage when the energy is stored in the magnetic element. The switches S_1, S_2, S_3 and S_4 are allowed to conduct.

Second stage (t_1, t_2): The switches S_1 and S_4 are gated off in t_1 . The capacitors C_{S1} and C_{S4} begin to charge with

the primary peak current. That's why this stage is very short in time.

Third stage (t_2, t_3): At t_2 , the voltage over C_{S1} and C_{S4} reaches $E/2$. Then the diodes D_{C1} and D_{C2} clamp the $E/2$ voltage on S_1 and S_4 switches. The voltage on the primary side of the transformer is zero. A freewheel path is formed by $L_{pri}, D_{C1}, D_{C2}, S_2$ and S_3 .

Fourth stage (t_3, t_4): The switches S_2 and S_3 are gated off in t_3 . The capacitors C_{S2} and C_{S3} are now charged with a current quite small than that of the second stage.

Fifth stage (t_4, t_5): When the voltage on the secondary side reaches the output voltage V_O , the diode D_O is set to conduct. The voltage on the primary side of the transformer stays in nV_O , where n denotes the turn ratio. A restriction on the design is now stated. If the reflected output voltage on the primary is made greater than the input voltage E , no energy is transferred to the load.

Sixth stage (t_5, t_6): After the energy stored in the magnetic field is completely delivered to the load, the secondary current goes to zero. The parasitic capacitances and inductances on the primary state a resonant circuit, with small oscillations of the current and the voltages.

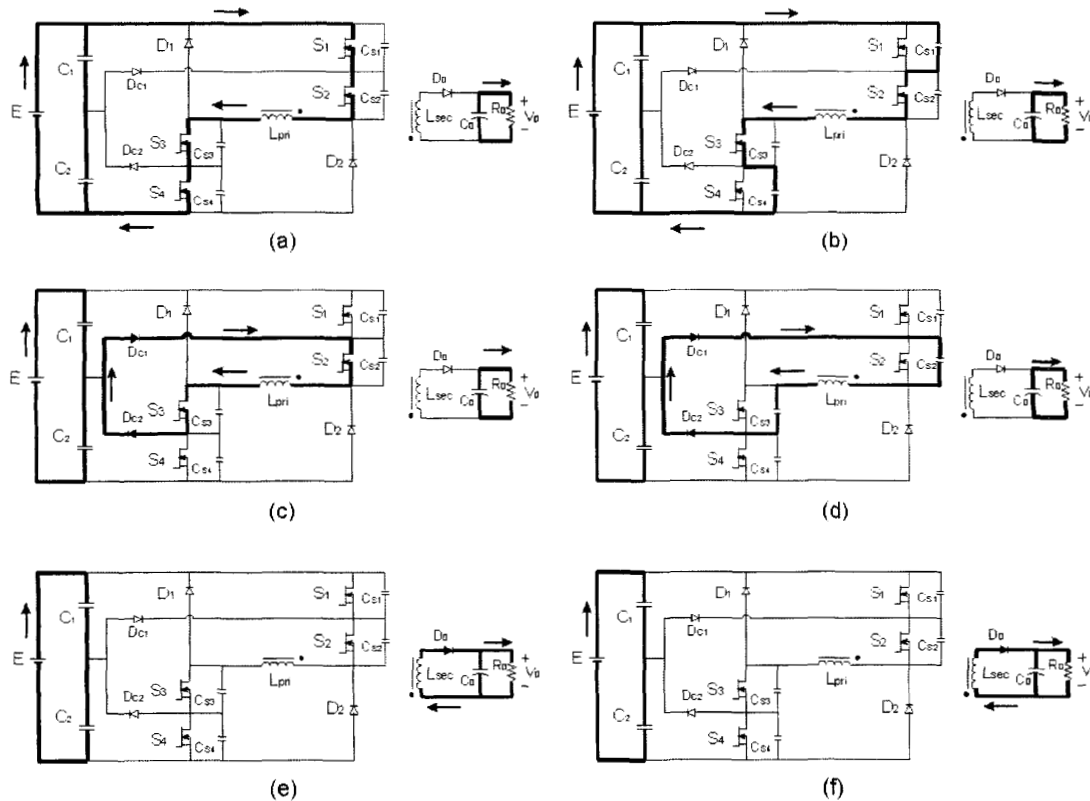


Fig. 2 – The topological stages of operation: (a) first stage; (b) second stage; (c) third stage; (d) fourth stage; (e) fifth stage and (f) sixth stage.

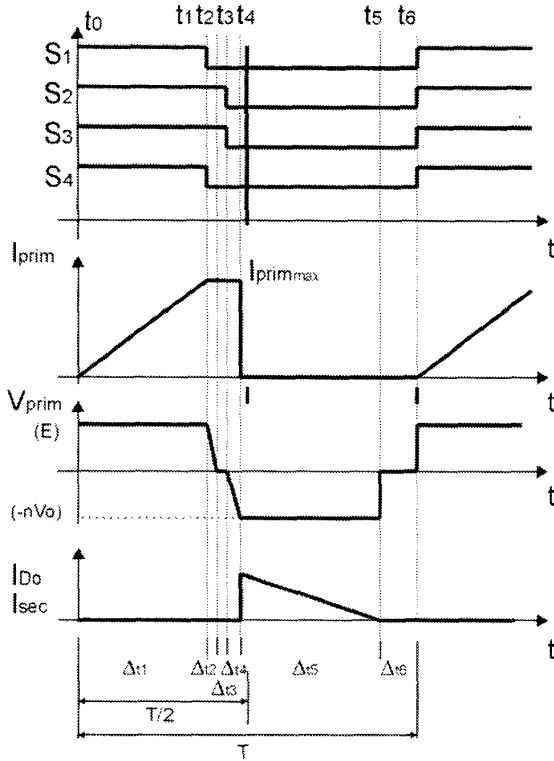


Fig. 3 – Main theoretical waveforms.

C. Output Characteristic

The output characteristic of the three level *flyback* converter could be obtained as the classical *flyback*. Since it delivers power in the same manner, this converter has the same output characteristic.

Starting with the principle that the output power is the same as the input, the development of the equations could be stated in a simple way. It was considered that the converter operates in a discontinuous mode of operation, for questions of stability [11].

The output mean voltage is then represented by the equation (1), where E denotes the input voltage, R_o the load resistor, L_{prim} the stored inductance referred to the primary, and f_s the switching frequency.

$$V_o = ED \sqrt{\frac{R_o}{2L_{prim}f_s}}$$

(1)

This equation also represents the output characteristic of the *buck-boost* converter in the discontinuous mode, from which the *flyback* is derived.

The duty cycle D is defined by the conducted time over the switching period (equation (2)), where t_c is the switching conducted time defined by $(t_1 - t_0)$, T is the switching period.

$$D = \frac{t_c}{T}$$

(2)

To state the equation (1) the second, third and fourth stages was not considered. These stages can be considered as very short, and does not contribute significantly to the output characteristic.

III. THE INPUT VOLTAGE BALANCE

The input capacitors voltage equilibrium is critical, because any difference in the on-times, or in intrinsic characteristics will lead the sharing voltage on the input capacitors to an unequal division.

This problem could be turned round splitting the primary side of the transformer in two coupled windings, with a one by one turns rate. This division does not change the converter principle of operation, but turns the equilibrium stable. Some current surge could happen, but these peaks are limited by the series resistance of the primary winding (since it is a high voltage winding with the number of turns in direct proportion with the voltage). Fig. 4 shows this division.

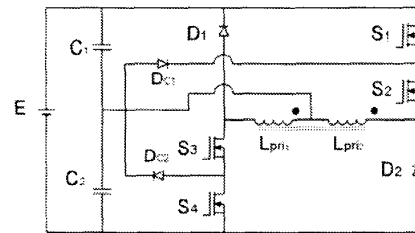


Fig. 4 - The split of the primary side to the equilibrium.

IV. EXPERIMENTAL RESULTS

To demonstrate the converter principal of operation, a 80W, 300-1200Vdc input prototype was initially constructed. This prototype has seven outputs, one 5Vdc regulated, one 24Vdc, another six 15Vdc, and another output working also for self source and for feedback regulation.

The voltage imposed on the primary winding of the transformer is presented in Fig. 1. The positive 400Vdc can be observed, and it is applied when all the switches are able to conduct.

On the off time, this voltage is inverted by the winding in a short period of time to dissipate currents stored in parasitic inductances. As this time ends, the voltage stays in a oscillating operation, caused by parasitic capacitances and inductances.

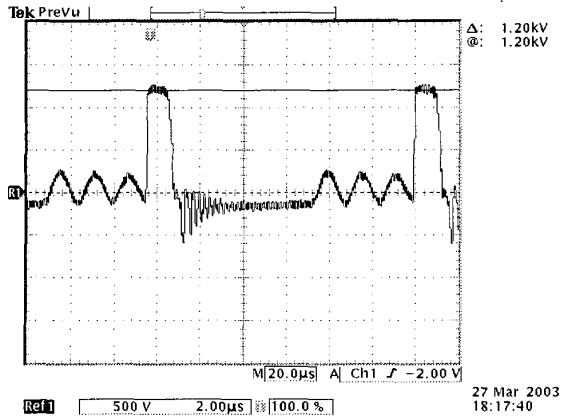


Fig. 5 – Total primary winding voltage.

In order to guarantee the input voltage balance between the input capacitors, a split on the primary winding was made. By the way, the voltage over the two primary winding is the same, and can be observed on Fig. 6, certifying the balance on the input capacitors.

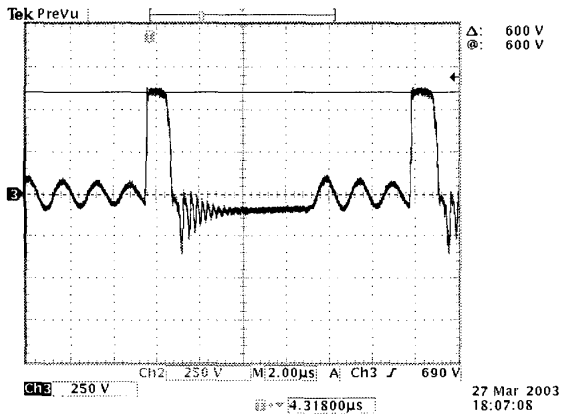


Fig. 6 – The primary winding voltages split on the first (Ch2) and second (Ch3) windings.

Another main characteristic of this converter is presented in Fig. 7 and Fig. 8. These pictures presents the drain to source voltages on the switches. It is showed that these voltages are clamped at 600V, half of the input voltage. The time delay between the external and internal switches setting off can be identified also. It could be observed at this picture that the voltage stress on the internal switches is lower than the external ones.

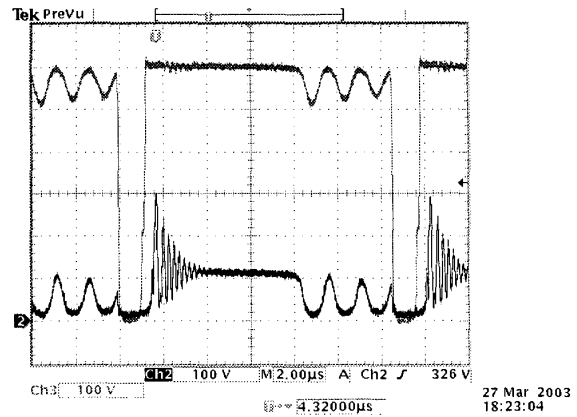


Fig. 7 – Drain to source voltages on S_1 (Ch3) and S_2 (Ch2) MOSFETs.

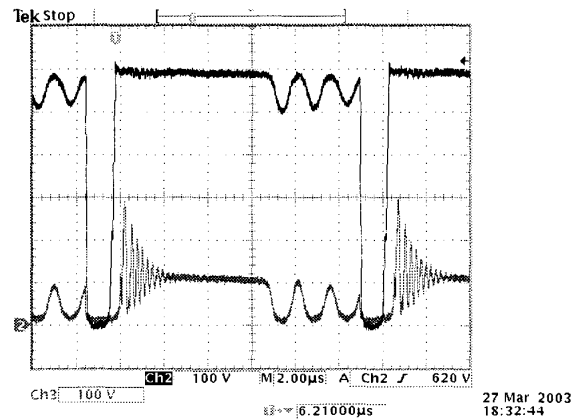


Fig. 8 – Drain to source voltages on S_3 (Ch3) and S_4 (Ch2) MOSFETs.

A zoom on the rise time could be observed in Fig. 9. This picture denotes that the clamping on the drain to source switches at 1200V input is efficient.

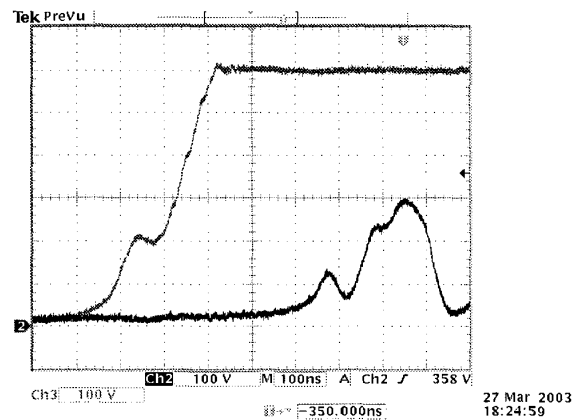


Fig. 9 - Drain to source voltages on S_1 (Ch3) and S_2 (Ch2) MOSFETs zoom on the rise time.

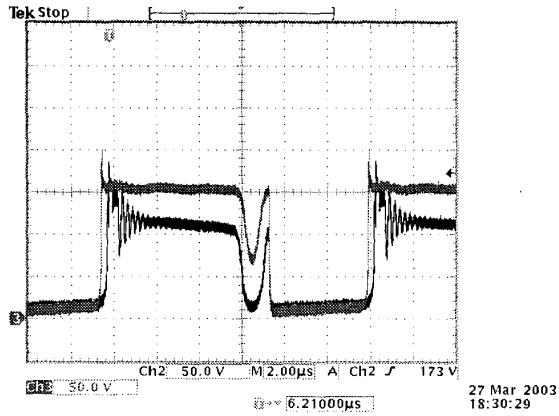


Fig. 10 – Drain to source voltages on S_1 (Ch3) and S_2 (Ch2) MOSFETs for a 300Vdc input.

The clamping voltage for a 300Vdc input is presented in Fig. 10. An over voltage could be observed here, caused mainly by the increase of the primary current on parasitic inductances [10]. At this low voltage, the clamping value of the switches is nearest the same, but the reflected voltage on the internal MOSFETs plus the voltage on the external ones, does not surpass the input voltage.

One of the outputs is shown in Fig. 11. Channel 1 is the secondary winding voltage and channel 2 shows the voltage deliver to the load, filtered by the output capacitor.

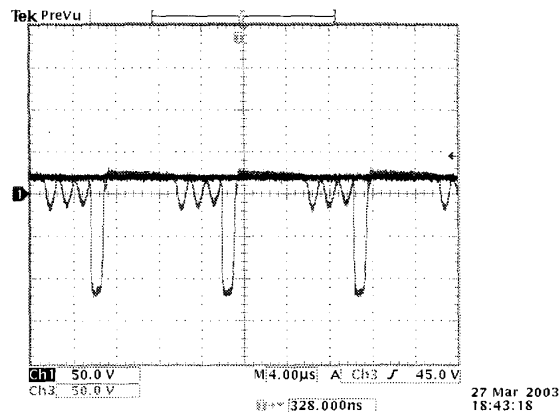


Fig. 11 – Output voltage (Ch1) and secondary winding voltage (Ch3).

V. CONCLUSIONS

A new three level flyback converter was presented. Its main characteristics, as low off-voltage stress and simplicity was demonstrated.

A first laboratory prototype was already constructed to demonstrate the operational principle. This was also intent to reach the objectives of voltage stress reduction on the switches.

Some considerations must be made on the clamping voltage on the switches. This voltage is clamped by the diodes in series with the input capacitors. As the primary winding and the layout path have some parasitic inductances, the voltage could not be clamped exactly on half of the input voltage. Some overshoot could be presented in this voltage. The value of this overshoot will depend on a good disposition of the components and the path in the layout. Also the characteristics of the clamping diodes could influence this overshoot value.

Finally, the main characteristic of the converter was proved. It was stated a new flyback converter that guarantees the reduction of the stress voltage on the switches. This converter has the same advantages of the classical flyback converters, but now available for high input voltages.

VI. REFERENCES

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