

## Single Phase Active Power Filter Controlled with a Digital Signal Processor – DSP

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**Abstract** - This paper presents a 1kVA single-phase active power filter (APF) digitally controlled, for the loads current harmonic distortion compensation as well as for the fundamental loads current displacement factor compensation. The APF is controlled using a Digital Signal Processor (DSP). Experimental results validate the analysis and design.

### I. INTRODUCTION

Active power filters (APF) are connected to the AC Mains to eliminate voltage distortion and/or load current harmonic distortion.

The parallel APF is used to compensate for the loads current harmonic distortion. It is connected in parallel with the AC mains and the load. The harmonics circulate through the APF, so that only the fundamental load current circulates through the AC Mains, resulting in a high power factor. The APF losses are usually low because only the harmonics currents circulate through it.

It is important to emphasize that the parallel APF does not change the load (its voltage and current are still the same) and if the APF fails the load is fed through the AC Mains, however, with a low power factor. Depending on the control strategy the APF also compensates for the fundamental load current displacement factor.

### II. ACTIVE POWER FILTER TOPOLOGY AND CONTROL STRATEGY

The Full-Bridge voltage source inverter (FB-VSI) shown in Fig. 1 is used as the APF. It is connected in parallel to the AC Mains through a coupling inductance  $L_f$ . The DC Bus is connected to a capacitor filter  $C_f$ , and its voltage must be kept constant and higher than the input voltage.

The control strategy is based on the input current sensor. This control strategy was chosen because it is very simple (it is not necessary to calculate the loads current harmonic components) and effective. The voltage and current control loops are described as follows:

**Voltage Control Loop (APF DC Bus voltage):** The DC Bus voltage must be kept constant and must be higher than the AC Mains voltage. This control loop is very slow because it composes the sinusoidal reference current, multiplying a sample of the AC Mains voltage.

**Current Control Loop:** This control loop makes the APF compensate for the loads current harmonic distortion, imposing a sinusoidal current in the AC Mains. This control loop is very fast to compensate for the harmonic currents.

The current control loop may use a hysteresis control, in which the switching frequency is variable, or the average current mode control technique, in which the switching frequency is constant. Because it makes the magnetic

components design easier, the average current mode control technique is chosen.

Fig. 1 presents the parallel APF with a block diagram of the control scheme, using the DSP. The current  $i_s$  and the voltages  $V_s$  and  $V_{Cr}$  are observed by the DSP to compose the control strategy.

The digital control was implemented using the TMS320LF2407 eZdsp DSK development kit by Texas.

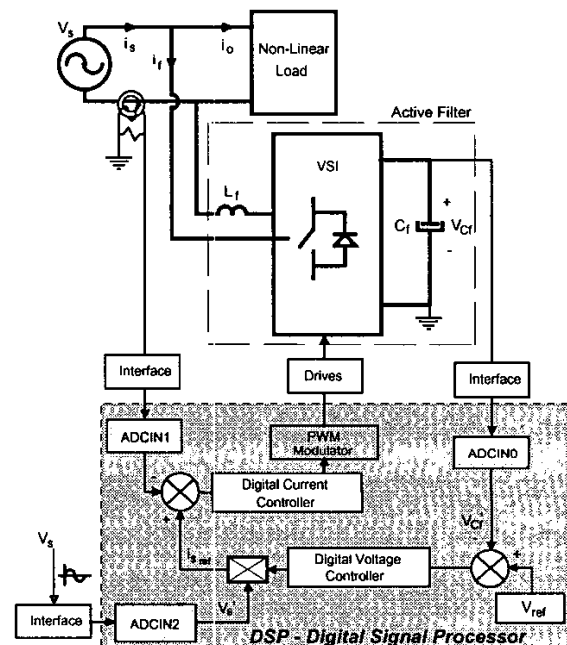


Fig. 1 – Parallel APF controlled through the sensor of the input current, using DSP.

### III. ACTIVE POWER FILTER DESIGN

The APF main specifications are presented in Table 1.

The APF coupling inductance  $L_f$  is calculated based on the parameterized current ripple (1), where  $M_i$  is the modulation index ( $M_i = V_{\text{peak}}/V_{Cr}$ ) [4]. For the presented specifications, the parameterized maximum current ripple is equal to 0,25.

$$\overline{\Delta i_f(t)} = \frac{2 \times \Delta i_f L_f}{V_{Cr} 2 \times f_s} = -M_i \text{sen} \omega t - (M_i \text{sen} \omega t)^2 \text{ for } \pi \leq \omega t \leq 2\pi \quad (1)$$

The expression to calculate the inductance  $L_f$  is given by (2).

$$L_f = \frac{\Delta i_{fmax} V_{Cf}}{\Delta i_{fmax} 2 \times f_s} = 750 \mu F \tag{2}$$

Table 1  
APF Main Specifications.

Parameter	Value
APF Reactive Power	1.000VAR
AC Mains rms Voltage ( $V_{s,rms}$ )	127V
Line Frequency ( $f_{line}$ )	60Hz
Current Ripple (AC Mains)	20%
DC Bus Voltage Ripple	10%
Switching Frequency $f_s$	30kHz
DC Bus Voltage ( $V_{dc}$ )	300V

The controllers used for the current and the voltage control loops are the proportional integral one (PI). The controllers were designed on the Z domain, based on the root locus methodology (LGR). To project the discrete controllers directly in Z, it should be obtained the discrete model that it relates the output with the input samples. This model may be represented with the aid of computer tools. Fig. 2 shows the current loop block diagram, with all the gains to be considered in the current controller design.

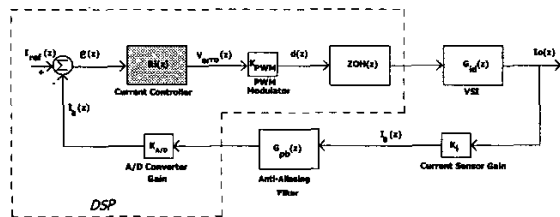


Fig. 2 – APF current control loop block diagram.

A. Current Controller Design

The methodology to design the discrete controller by the root locus is similar to the methodology used to design an analog controller. The difference is that the closed loop transfer function poles must be inside the unitary circle to ensure the system stability. And to ensure that the system natural oscillatory frequency, when submitted to the step, is smaller than the sample frequency, the poles should be inside the region presented in Fig. 3-a. If the oscillatory frequency is equal to the sample frequency, the system response will be as shown in Fig. 3-b.

The time of processing of the software was not represented in the open loop transfer function used in the MATLAB program, although it may not be disregarded. The considered time of processing is 1/4 of the sample frequency. Fig. 4 presents the phase of the time of processing of the discrete system.

To a cross-over frequency of 5kHz, the phase shift due to the time of processing is already 15°, so it is recommended that the cross-over frequency be below 5kHz and that the phase margin be above 60°, because the time of processing is not being considered in the Z domain design. The compensator design criteria are presented in Table 2.

The APF closed loop transfer function root locus with the digital controller is presented in Fig. 5. It may be observed that the root locus is inside the desired region, according to Fig. 3-a. Fig. 6 shows the open loop transfer function phase Bode diagram. The open loop transfer function parameters

as well as the current controller parameters are presented in Table 3.

Fig. 7 shows the open loop transfer function step response, with the compensator parameters presented in Table 3. As may be noticed there is no overshoot or oscillations.

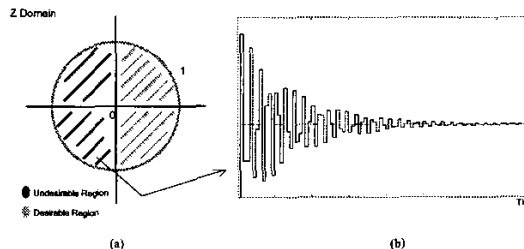


Fig. 3– (a) Closed loop transfer function poles desirable location. (b) System natural oscillatory frequency equal to the sample frequency.

Table 2  
Current Controller Design Criteria.

Parameter	Obtained by the Root Locus
Cross-Over Frequency	5 kHz
Phase Margin	60°
Pole Frequency	30 kHz ( <i>anti-aliasing filter</i> )
Zero Frequency	3,75 kHz

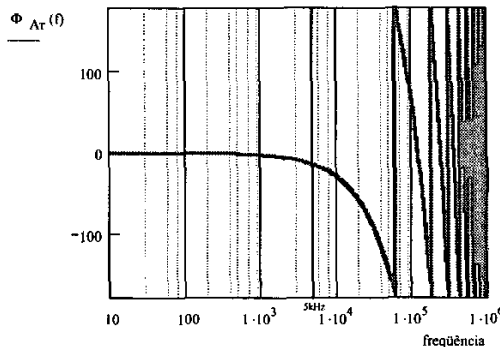


Fig. 4 –Discrete system time processing phase.

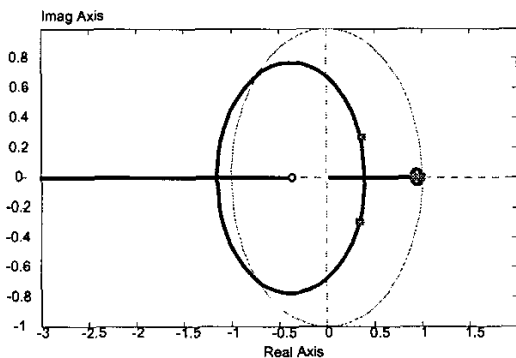


Fig. 5– APF closed loop transfer function root locus, with the digital controller.

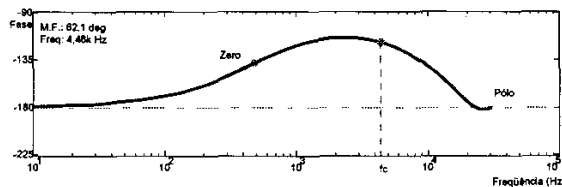


Fig. 6– APF open loop transfer function phase, with the digital controller.

Table 3  
Current Controller Parameters.

Parameter	Value obtained by the root locus
Cross Over Frequency	4,46 kHz
Phase Margin	62,1°
Pole Frequency	30 kHz (anti-aliasing filter)
Zero Frequency	500 Hz
Static Gain $K_{Ri}$	75

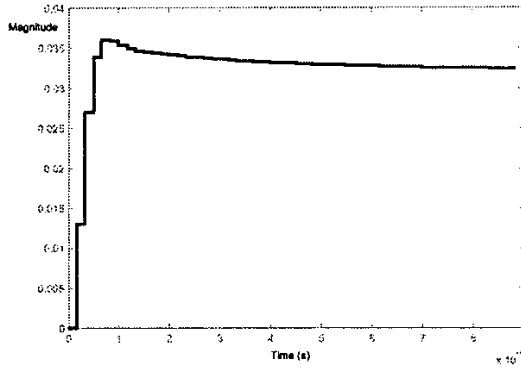


Fig. 7 – Step response.

The following controller were obtained in the Z domain:

$$R_i(z) = 75 \times \left( \frac{1 + 0,95z^{-1}}{1 - z^{-1}} \right) \quad (3)$$

**B. Voltage Controller Design**

To design the voltage controller in the Z domain the same methodology employed for the current controller is used. The only difference is that the voltage controller must be slow, so the cross over frequency is about 1/30 of the line frequency. The closed loop transfer function root locus is presented in Fig. 8 and its phase in Fig. 9.

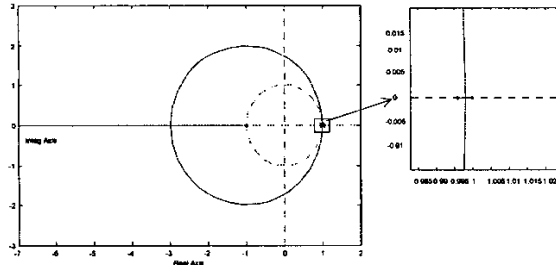


Fig. 8– Closed loop transfer function root locus.

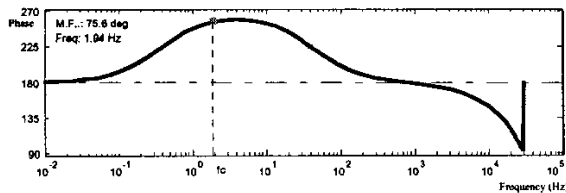


Fig. 9 – Open loop transfer function phase.

The open loop transfer function and the voltage controller parameters are presented in Table 4.

Table 4  
Voltage Controller Parameters.

Parameter	Value obtained by the root locus
Cross Over Frequency	2 Hz
Phase Margin	75,6°
Pole Frequency	60 Hz (anti-aliasing filter)
Zero Frequency	4 Hz
Static Gain $K_{Ri}$	0,1

The following controller were obtained in the Z domain:

$$R_v(z) = 0,1 \times \left( \frac{1 + 0,995z^{-1}}{1 - z^{-1}} \right) \quad (4)$$

**IV. EXPERIMENTAL RESULTS**

A 1kVar APF model was built. The main parameters are as follows:  $V_{s,rms}=127V$ ,  $f_{line}=60Hz$ ,  $V_{Cr}=300V$ ,  $f_s=30kHz$ ,  $C_f=1.88mF$ ,  $L_f=750\mu H$ .

The APF was tested with the non-linear load presented in Fig. 10, which presented a total harmonic current distortion of 34.27% and a current phase displacement of 13°, resulting in a power factor of 0.92.

The experimental results are presented in Fig. 12. It may be observed the AC mains voltage, the distorted load current, the APF current, compensating the harmonic distortion, and the resulting input current, which is sinusoidal and in phase with the AC mains voltage. In table 5 is presented the current harmonic distortion, the current phase displacement and the resulting power factor for the load and the input current. The load current harmonic distortion was reduced from 32.27% to 5.72%, due to the APF. The power factor was increased from 0.92 to 1, and the current phase displacement was reduced from 13° to 1°. This indicates that the APF controlled by the DSP is working as expected, and the voltage and current control loops are designed properly.

If a faster current control loop were used, which is possible increasing the switching frequency and/or the sample frequency, the APF performance would improve, which means that an even smaller input current harmonic distortion would be obtained.

Table 5  
Load and AC Mains Current Harmonic Distortion and Power Factor.

Load			AC Mains			
THD <sub>i</sub>	PF	$\phi^\circ$	THD <sub>v</sub>	THD <sub>i</sub>	PF	$\phi^\circ$
34.27%	0.92	13	2.82%	5.72%	1	1

The APF was also tested with the linear load of Fig. 11. As may be observed in Fig. 13 the load current is sinusoidal, however, has a phase displacement (48°). In this case the APF would not generate any harmonic components, and so its current should have a 90° displacement factor in relation with the AC mains voltage, indicating that the APF is processing only a reactive power, as may be observed in Fig. 13. The resulting input current is in phase with the AC mains voltage. As a high frequency filter was not used, harmonics due to the switching frequency are observed in the resulting input current.

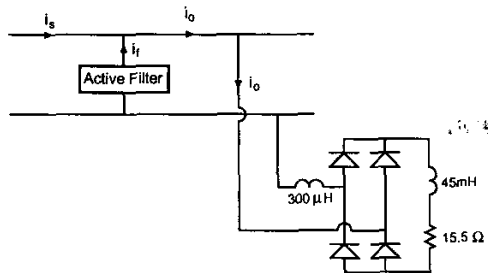


Fig. 10 – Non-linear load.

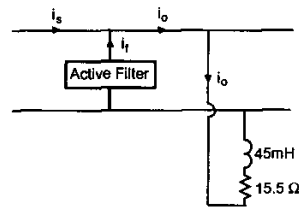


Fig. 11 – Linear Load.

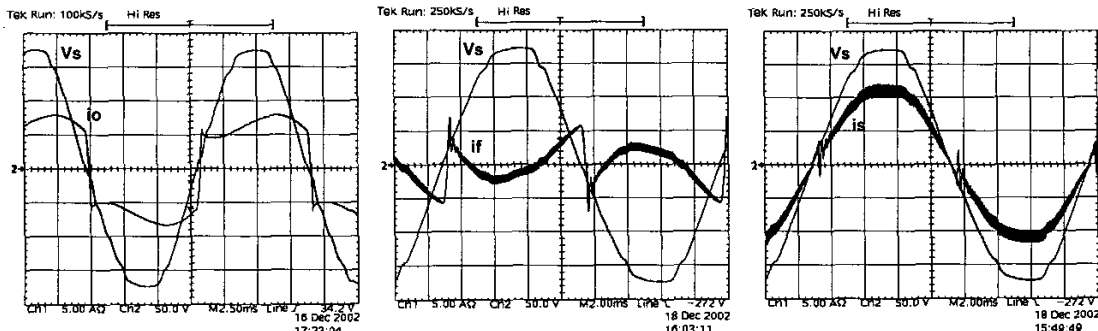


Fig. 12 – AC mains voltage (50V/div.), load current (5A/div.), APF current (5A/div.) and the resulting input current (5A/div.), for the non-linear load.

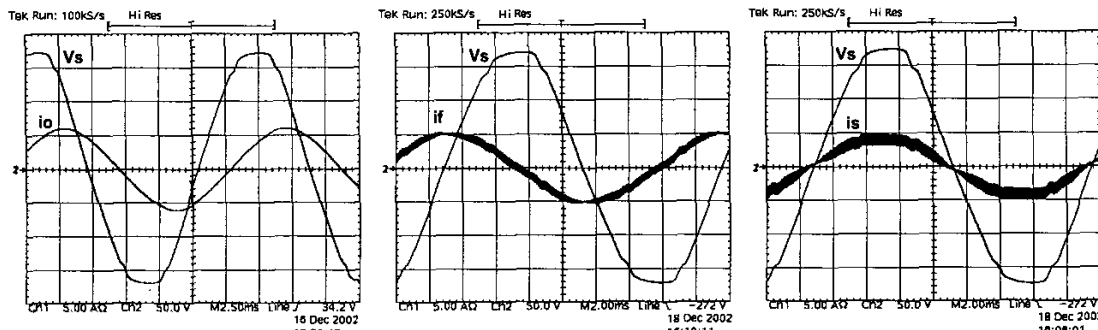


Fig. 13 – AC Mains voltage (50V/div.), load current (5A/div.), APF current (5A/div.) and the resulting input current (5A/div.), for the linear load.

V. CONCLUSION

In this paper a single-phase active power filter controlled by a digital signal processor is presented. The APF is controlled through the sensor of the input current, which is a very simple and effective technique.

Experimental results of the APF compensating a non-linear and a linear load validate the analysis. The APF performance to compensate harmonic currents could be improved if a faster current control loop were used, which is possible increasing the switching frequency and/or the sample frequency.

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