BUCK CONVERTER WITH ZVS THREE LEVEL BOOST CLAMPING

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***Abstract* – This work presents the study of a three level DC-DC resonant buck converter with boost active clamping, soft switching (ZVS - Zero Voltage Switching) and constant frequency PWM (pulse width modulation). The main advantages of this topology are high efficiency and lower voltage stress on the switches when compared to buck converters with two level boost clamping.**

I. INTRODUCTION

The use of resonant converters with ZVS has the main objective of reducing switching losses, which allows operation at higher frequencies. However, the main disadvantages of resonant converters [2 and 3] are copper losses and higher voltages across the switches. Also, the wider the load variation in these converters, the larger the amount of reactive energy required to maintain the ZVS commutation. The larger amount reactive energy increases the current of the auxiliary DC bus. This work focuses on reducing the voltage across the active switches and proposes a structure with a large number of levels.

An initial study of DC-DC multilevel converters with soft commutation (ZVS), active clamping and constant frequency PWM was carried out. The objective of this work is the study of the DC-DC buck converter with three level boost active clamping. Compared to the ZVS two level buck converter, the main advantage of three level topologies is the 50% reduction of the voltage applied across the active switches. References [2 and 3] studied several families of two level DC-DC ZVS PWM converters with active clamping. These converters present characteristics similar to classic PWM converters as the amount of reactive energy consumed by them decreases. Among these families of converters, the buck converter with two level boost clamping, as shown in Fig. 1, was analyzed in references [2 and 3].

The DC-DC buck converter was chosen due to the possibility of using it in applications where the input voltage is relatively high and it is necessary to spread the voltage stresses among the active switches. When low switching losses and low emissions of electromagnetic noise are requirements, it is desirable to operate the converter with ZVS. However, resonant converters increase the voltage of the auxiliary DC bus in relation to the input voltage.

Limited work has been done on non-isolated two level DC-DC converters with ZVS, which is the reason for the few number of references [2, 3, 4] in this paper. The buck converter with two level boost clamping was presented [2, 3]. The study of two level DC-DC ZVS converters is the basis for the study of topologies of three or more levels with ZVS. References [1, 3] also presented topologies of three level DC-DC converters, which aimed to reduce the voltage across the transistors, but these topologies operate with dissipative commutation. A study to reduce the voltage stress of the diodes through a diode association was presented in [5].

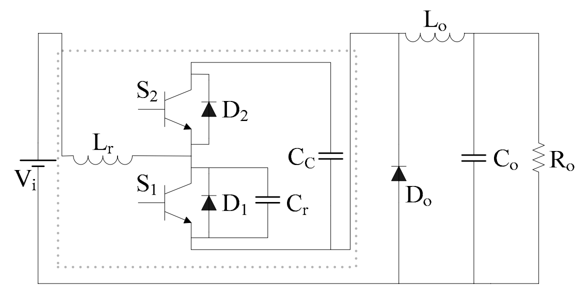

Fig. 1 – Buck with two level ZVS boost clamping.

II. BUCK CONVERTER WITH THREE LEVEL BOOST CLAMPING

Fig. 2 shows the commutation cells of the buck converter with three level boost clamping.

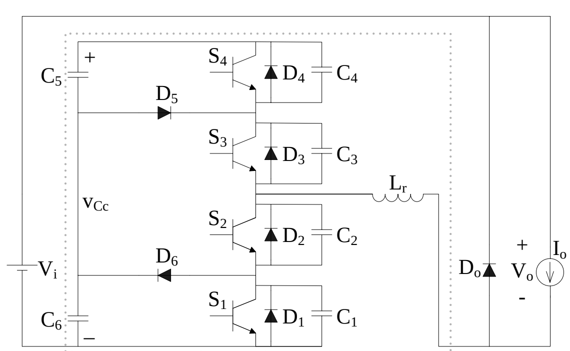

Fig. 2 – Buck converter with three level ZVS boost clamping.

For the initial study of the two and three level topologies, the following considerations are made:

- The converter operates in steady state;
- The switches are considered ideal;
- The converter output inductor is large, thus the load can be represented by a constant current source;

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- Inductor L_r stores enough energy to complete the charge and discharge of the resonant capacitors (C_1, C_2, C_3 and $C_4 = C_r$) and polarize the diodes in parallel with the switches;
- The resonant frequency produced by L_r and the auxiliary bus capacitance ($C_c \approx (C_5+C_6)/2$) is much lower than the frequency of the resonant circuit formed by L_r and C_r. In other words, the auxiliary bus capacitance, C_c, is much larger than C_r. Thus, the capacitor of the auxiliary DC bus can be represented by a constant voltage source.

To facilitate the converter analysis, Fig. 2 can be redrawn as shown in Fig. 3.

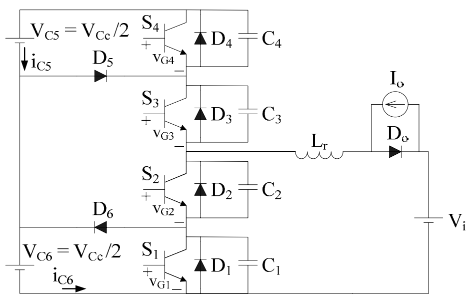

Fig. 3 – Redrawn buck converter with boost clamping.

A. Operation Stages

Fig. 4 shows the drive signals, the currents and the voltages of the switches, considering that the voltages across capacitors C_5 and C_6 are balanced and that at t_3 the voltage across capacitor C_1 reaches $V_{Cc}/2$ and at t_8 the voltage across capacitor C_4 reaches $V_{Cc}/2$. Even if the conditions above are not satisfied, the converter will operate with ZVS, but with a little difference in the waveforms and operation modes.

The necessary condition for zero voltage switching (ZVS) is to drive each switch when the capacitor in parallel with the switch is discharged. In other words, to avoid dissipative commutation, or hard switching, the drive signals for switches S_1 and S_2 (V_{G1G2}) should start between t_{10} and t_{13} and for switches S_3 and S_4 (V_{G3G4}) should start between t_4 and t_7.

The converter's operation stages presented in Fig. 4 take into consideration the abovementioned restrictions.

Fig. 4 presents the converter's main waveforms, from which each of the converter operation intervals are described.

1^{st} Stage [t_1-t_2] – Switches S_1 and S_2 are conducting. The current through inductor L_r is positive, constant and equal to I_o. Diode D_o is not polarized.

2^{nd} Stage [t_2-t_3] – Switch S_1 is turned off, but S_2 is still conducting. The current is divided among resonant capacitors C_1, C_3 and C_4. In other words, the current through inductor L_r is equal to I_o of which 2/3 circulates through C_1 and 1/3 through C_3 and C_4. The voltage across capacitor C_1 increases from zero to V_x, which is lower than $V_{Cc}/2$, and the voltages across C_3 and C_4 decrease from $V_{Cc}/2$ to ($V_{Cc}/2 - V_x/2$). Voltage V_x depends on the interval between the turn off of switches S_1 and S_2.

3^{rd} Stage [t_3-t_4] – Switch S_2 is turned off and the current through the four resonant capacitors is $I_o/2$. When the voltage across capacitor C_1 reaches $V_{Cc}/2$ the 4^{th} stage begins.

4^{th} Stage [t_4-t_5] – A division of current occurs like in the second stage. The next stage starts when the voltages across capacitors C_3 and C_4 reach zero.

5^{th} Stage [t_5-t_6] – Diodes D_3, D_4 and D_o are polarized. D_3 and D_4 conduct the current through inductor Lr.

6^{th} Stage [t_6-t_7] – The resonant inductor current becomes negative and switches S_3 and S_4 start to conduct.

7^{th} Stage [t_7-t_8] – In this stage S_4 is turned off and the voltage across C_4 increases from zero to V_x, which is lower than $V_{Cc}/2$, and depends of the interval between the blocks of S_3 and S_4. When switch S_3 turns off the 8^{th} stage begins.

8^{th} Stage [t_8-t_9] – The current through the four resonant capacitors is $I_o/2$. This stage ends when the voltage across C_4 reaches $V_{Cc}/2$.

9^{th} Stage [t_9-t_{10}] – In this stage diode D_5 is polarized and the voltage across C_3 continues to increase until it reaches $V_{Cc}/2$.

10^{th} Stage [t_{10}-t_{11}] – Diodes D_1 and D_2 are polarized and conduct the resonant inductor current.

11^{th} Stage [t_{11}-t_1] – This stage begins when the resonant inductor current becomes positive. Switches S_1 and S_2 conduct the resonant inductor current, which increases until reaches I_o, initializing the first stage of the operation again.

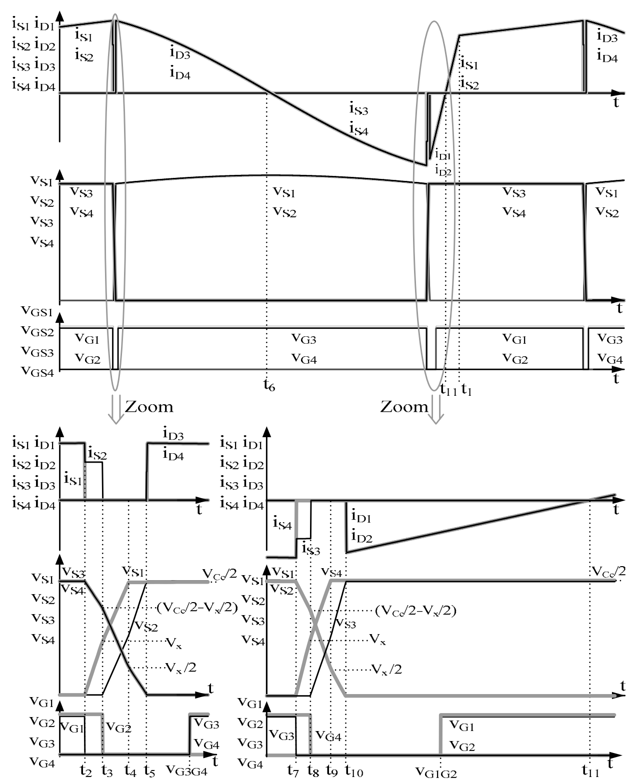

Fig. 4 – Main waveforms of the buck converter with three level ZVS boost clamping.

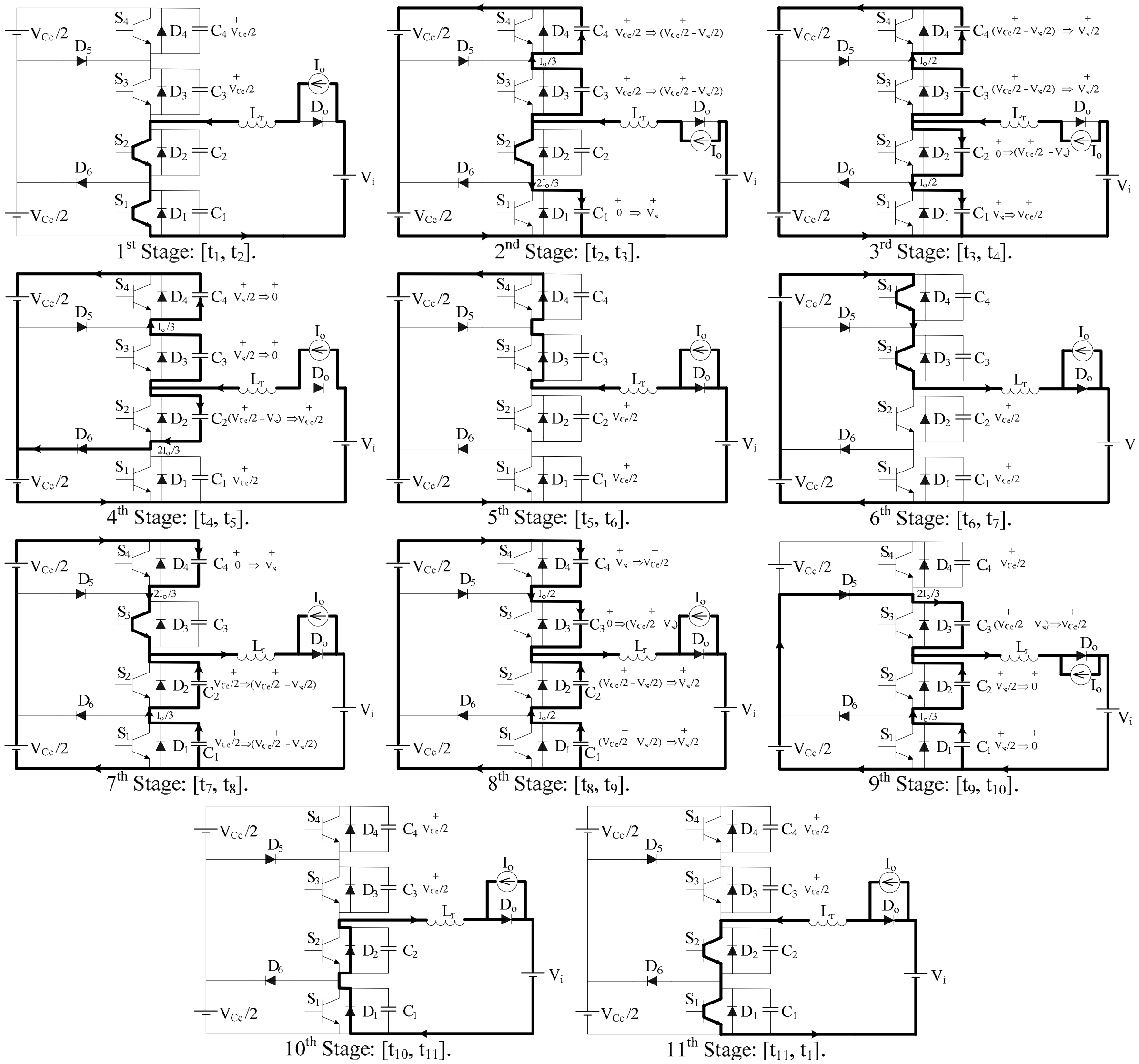

Fig. 5 – Operation stages of the buck converter with three level ZVS boost clamping.

B. Static Transfer Characteristic

To simplify the calculation of the static transfer characteristic, the very short intervals between t_2 and t_5 and between t_7 and t_{10} are ignored. Fig. 4 is redrawn, as presented Fig. 6, for the analysis.

In this figure duty cycle "D" is defined as the interval between the turn off of switches S_3 and S_4 and the turn off of switches S_1 and S_2. This is feasible because the switches do not need to be driven complementarily.

Using these approximations, the static transfer characteristics of the buck converter with two and three level boost clamping are the same.

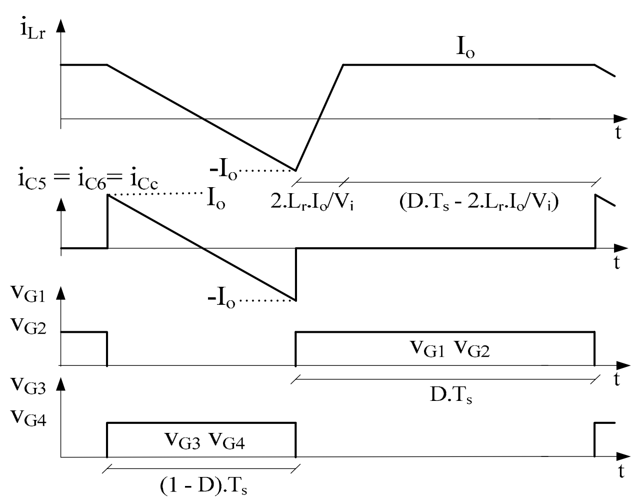

Fig. 6 – Simplified waveforms of the buck converter with three level active boost clamping.

The initial current through capacitors C_5 and C_6 is I_o. The currents through these capacitors, i_{Cc}, is described by (1).

$$i_{C5}(t) = i_{C6}(t) = i_{Cc}(t) = I_o - \frac{(V_{Cc} - V_o)}{L_r}.t \qquad (1)$$

The average value of (1) is zero because the system is stable. Thus, by integrating (1), the expression of the auxiliary DC bus voltage (V_{Cc}) is obtained.

$$V_{Cc} = \frac{2L_r I_o}{T_s(1-D)} + V_i \qquad (2)$$

To study the converter the following variables are defined:

$\beta = \frac{V_{Cc}}{V_o}$ ⇒ Relationship between the auxiliary DC bus voltage and the output voltage, (3)

$q = \frac{V_o}{V_i}$ ⇒ Relationship between output voltage and the input voltage, (4)

L_n ⇒ Normalized inductance.

The normalized inductance, L_n, is dimensionless and was defined as a function of the input voltage, output current and commutation period, as presented in (5).

$$L_n = L_r \frac{I_o}{V_i T_s} \qquad (5)$$

To calculate β, (2) and (5) are substituted into (3).

$$\boxed{\beta = \frac{V_{Cc}}{V_o} = \frac{2L_n}{(1-D)} + 1} \qquad (6)$$

Equation (6) is used to plot β for different values of duty cycle "D".

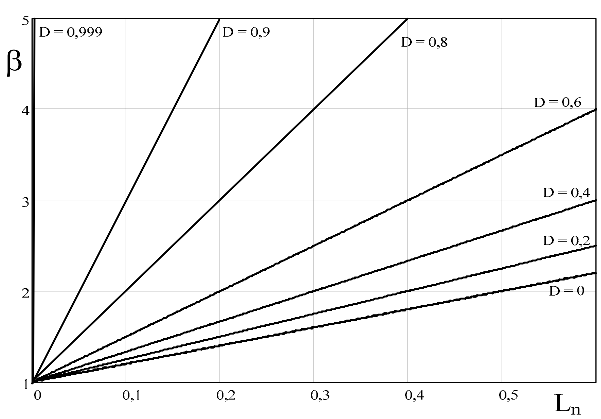

Fig. 7 – Normalized voltage of the auxiliary bus.

The highest voltage across switches S_1 and S_2 of the buck converter with two level clamping is equal to the auxiliary DC bus voltage V_{Cc}. For the converter presented in Fig. 3 but with three level clamping, the highest normalized voltage applied to the switches is equal to $V_{Cc}/2$. From Fig. 7, the smaller the normalized resonant inductance (L_n), the lower the voltage across the auxiliary bus is.

The static transfer characteristic is calculated from (7). It is obtained from the sum of the voltages considering the system stable, because the average values of the voltages across inductors L_r and L_o are zero. The relationship between voltages V_{Cc} and V_i is

$$V_o = V_i - (1-D)V_{Cc} \qquad (7)$$

By substituting (6) into (7), (8) is obtained

$$\boxed{q = D - 2L_n}. \qquad (8)$$

Fig. 8 presents the static transfer characteristic of the buck converter with three level boost clamping for different values of duty cycle "D".

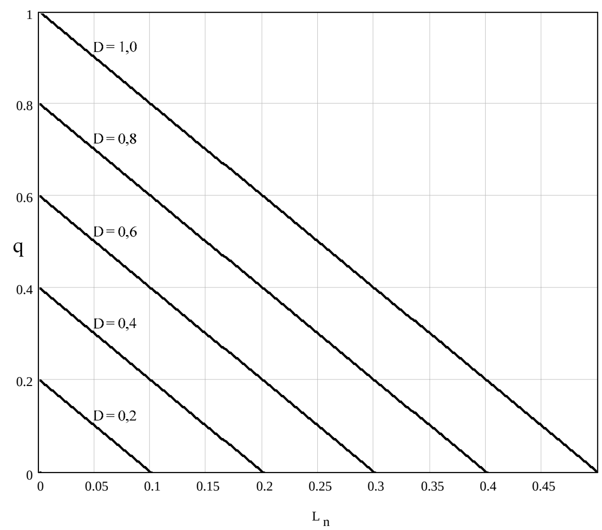

Fig. 8 – Static transfer characteristic.

C. Design

The following specifications were considered for designing the circuit components:

V_i = 500V ⇒ Input voltage
f_s = 20kHz ⇒ Switching frequency
V_o = 150V ⇒ Output voltage
P_o = 1kW ⇒ Output power
ΔV_o = 1% ⇒ Output voltage ripple
ΔI_o = 30% ⇒ Input current ripple
ΔV_{Cc} = 7% ⇒ Bus voltage ripple
C_r = 4.7nF ⇒ Resonant capacitance C_r (C_1, C_2, C_3 and C_4)
η = 0.96 ⇒ Efficiency

In order to choose an adequate value for the resonant inductance, some drive adjustments should be made. The drive signals of switches S_1 and S_2 can be applied right after resonant capacitors C_1 and C_2 discharge, but these drive signals should be applied before the current of inductor L_r becomes positive in order to avoid dissipative commutation. For a better safety margin for the drive circuitry, an inductance of 52 µH was chosen. The minimum inductance for this design is approximately 30 µH, but this value would be difficult to adjust for a considerable load variation and the converter would end up operating without ZVS.

$$L_r = 52\ \mu H \Rightarrow L_n = 0.014$$

The duty cycle is calculated isolating D from (8).

$$D = \frac{V_o}{V_i} + 2.L_n \ \Rightarrow \ D = 0.328$$

The output current and the output resistor are calculated by

$$I_o = \frac{P_o}{V_o} = 6.67\,A$$

$$R_o = \frac{V_o^{\ 2}}{P_o} = 22.5\,\Omega$$

The output capacitor is calculated as in the case of a traditional buck converter.

$$C_o = \frac{V_i}{f_s^{\ 2}.\Delta V_o.V_o.\pi^3.L_o} \ \Rightarrow \ C_o = 8.6\,\mu F$$

Due to the current capability specified by the capacitor manufacturers, $\boxed{C_o = 235\,\mu F}$ was chosen.

The input inductance can be calculated from the current variation in interval t_{1_2}.

$$L_o = \frac{(V_i - V_o).t_{1\_2}}{I_o \Delta I_o} \Rightarrow L_o = \frac{(V_i - V_o)}{I_o \Delta I_o}.\left[\frac{D}{f_s} - \frac{2.I_o.L_r}{V_i}\right] \Rightarrow$$

$$\boxed{L_o = 2.6mH}$$

Integrating the current through capacitors C_5 and C_6 and using the design specifications and voltage ripples across these capacitors (ΔV_{Cc}), the capacitances are calculated

$$C_5 = C_6 = \frac{I_o.(1-D)}{\Delta V_{Cc}.f_s} - \frac{(V_{Cc} - V_i).(1-D)^2}{4.\Delta V_{Cc}.L_r.f_s^{\ 2}}$$

$$C_5 = C_6 = 3.1\mu F \ \Rightarrow \boxed{C_5 = C_6 = 3.3\mu F}$$

From (7) the average voltage of the auxiliary DC bus is defined as:

$$\overline{V_{Cc}} = \frac{V_i - V_o}{(1-D)} \Rightarrow \overline{V_{Cc}} = 520\,V$$

D. Experimental Results

The experimental results of the buck converter with three level boost clamping using the design presented in Fig. 9, are presented in Fig. 10 and Fig 11.

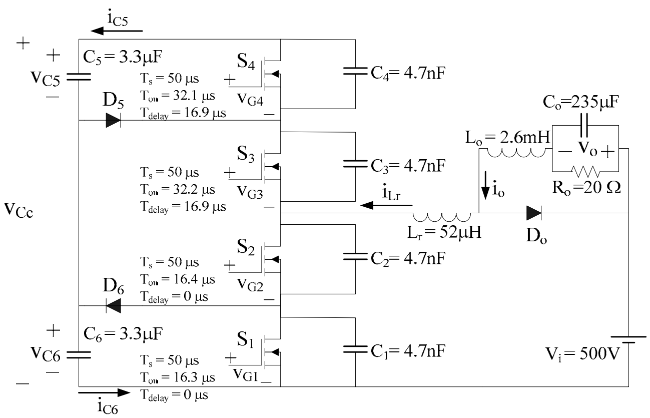

Fig. 9 – Circuit tested in the laboratory.

The prototype tested in the laboratory presented V_o = 142V, P_o = 1kW, $\Delta I_o \approx 0.3I_o$ and ΔV_o is much smaller than 1% because the output capacitor is oversized.

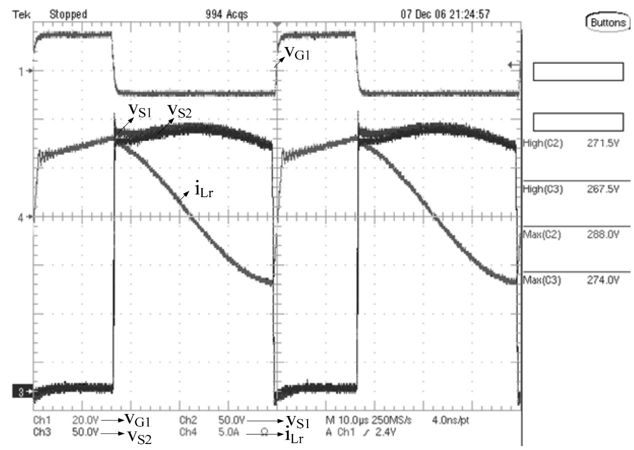

Fig. 10 – Voltage across switches S_1 and S_2, drive signal of S_1 and resonant inductor current.

In Fig. 10 voltage peak is observed across the switches, which is probably caused by parasitic inductance from the layout, and presents a maximum voltage peak equal to 288V (58% of V_i).

It was noted during the tests under rated power that all of the transistors operate with zero voltage switching (ZVS). The designed converter operates with ZVS from 100% to 70% of the rated power. Below 70%, only turn-on occurs under the zero voltage condition and the additional losses are compensated by less copper losses in the components. Fig. 12 shows the results for the efficiency tests under several load conditions.

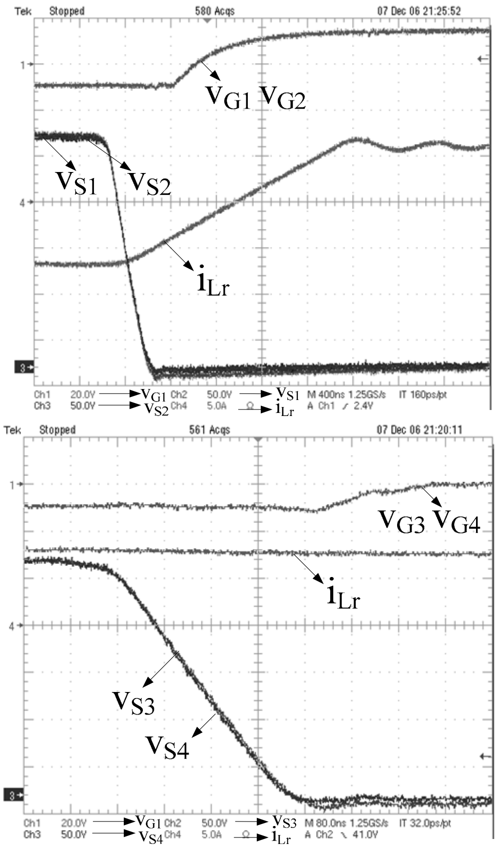

Fig. 11 – Zoom in of the turn off transient with zero voltage across the transistors.

In this design the voltages across capacitors C_5 and C_6, which define the voltage across the switches, are balanced over a wide input voltage range, from zero to V_i.

It was observed that, if the resonant capacitance were reduced, the load range, under which ZVS would occur, increases. However, this would make it difficult for the voltages across C_5 and C_6 to converge to values close to the input voltage.

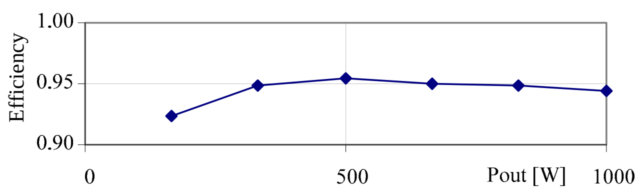

Fig. 12 – Converter efficiency.

III. Conclusion

The buck topologies with ZVS have the advantage of reduced commutation losses when compared to a traditional buck converter. Therefore, they operate with higher efficiency at higher frequencies.

Comparing the proposed topology with the buck converter with two level ZVS boost clamping [2, 3], the proposed topology presented a 50% voltage reduction across the switches. However, the three level converter has two additional bidirectional switches and capacitors to compose the auxiliary DC bus. For the two level converter, the voltage across the single bus capacitor is stable because this capacitor is subjected only to the bus voltage, which has a constant average value in steady state. For three or more level converters only the sum of the voltages across the bus capacitors is always stable in steady state, but the average voltage in steady state across each of these capacitors depends on the drive circuit parameters.

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