

# THREE-LEVEL HALF-BRIDGE INVERTER BASED ON THE THREE-STATE SWITCHING CELL

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**Abstract** – This paper presents a half-bridge three-level inverter, based on a commutation cell of three states. The principle of operation of this inverter is described and the main theoretical waveforms are presented, as well as the simulations and experimental results. The main expressions for the design of the inverter are also presented. This inverter presents the following advantages over the classic inverter: the frequency at the load is twice the switching frequency; the amplitude of the output voltage is half that of the classic converter; the load current is divided amongst the switches, therefore reducing the conduction losses. In light of its characteristics, we believe that inverter is appropriate for industrial applications.

**Index Terms** — half-bridge inverter, three-level inverter, three-state cell.

## I. INTRODUCTION

The advances in the power electronics have permitted the increasing usage of dc-ac converters, which transform the energy from a dc source into an ac source and, therefore, are referred to as inverters. The dc input power source can be, among others, a battery bank, photovoltaic solar panels, fuel cells, as well as the output of a rectifier.

Among their many applications, inverters are used for speed control of ac machines, inductive heating and uninterrupted power supply systems, which are becoming more and more popular in the industry.

Originally, dc-ac converters presented a rectangular output with high harmonic component, which is undesirable for many applications. To minimize this problem, inverters that employ pulse width modulation (PWM) are currently used.

In PWM converters, it is common to increase the switching frequency, so that the harmonic components are shifted to higher frequencies, making filtering easier. However, increasing the switching frequency is limited due to the increase in the switching losses.

In the multilevel converters, found in the literature, the voltage across the switches is reduced and the output voltage frequency is higher than the switching frequency. The output voltage of these inverters presents a lower harmonic content, when compared to the classic inverters.

In full-bridge inverters, besides increasing the frequency, it is also possible to use three-level modulation. This modulation makes the frequency of the output voltage twice the switching frequency. However, this modulation strategy can not be applied to the half-bridge inverters.

The proposed three-level half-bridge inverter is based on the three-state switching cell that was originally proposed for dc-dc converters [1]. DC-DC converters that use this cell present the following advantages: reduced conduction losses of the switches; the frequency of the reactive elements is twice the switching frequency; weight and volume reduction. These characteristics are also desirable for inverters.

The three-level half-bridge inverter based on the three-state switching cell presents the following advantages over the classic inverter: the frequency at the load is twice the switching frequency; the amplitude of the output voltage is half that of the classic converter; the load current is divided amongst the switches, therefore reducing the conduction losses.

## II. THREE STATE COMMUTATION CELL

In [1], several three-state commutation cells proposed for application in DC-DC converters, of which the so called “cell B” is of interest. It is composed of two switches, two diodes and a central tap transformer, as depicted on Fig. 1. This cell is the basis for the cell proposed in this paper.

The cell proposed in [1] presents unidirectional current flow thus, in order to apply it to inverters, it is necessary to make it bidirectional. This is easily achieved by replacing the diodes by controlled switches with anti-parallel diodes, as depicted in Fig. 2a.

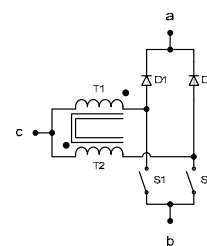


Fig. 1 - Unidirectional current three-state commutation cell.

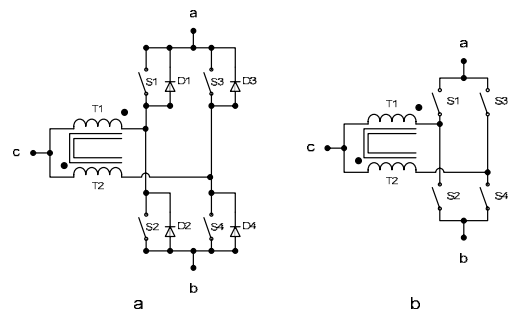


Fig. 2 - Bidirectional current three-state commutation cell.

To simplify the later analyze, one can consider the switches to be ideal, as shown in Fig. 2b. In this case the switches should be driven in a complementary fashion.

### A. Operating states

The commutation cell of classic inverters, shown on Fig. 3a, is defined as a two-state commutation cell because of the complementary operation of the switches; that is, when one switch conducts the other is blocked and vice-versa.

Fig. 3b illustrates the switching states of a two-state commutation cell. Note that there is a neutral state, in which none of the switches conduct, and no energy is transferred through this cell.

The three-state commutation cell proposed here has five possible configurations for the switches, as shown in Fig. 4. However, it should be stressed that one of these possibilities is the neutral state, in which no switch conducts, similar to the aforementioned two-state cell.

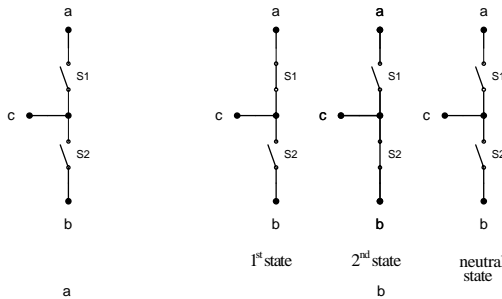


Fig. 3 - Switching states of a two-state commutation cell.

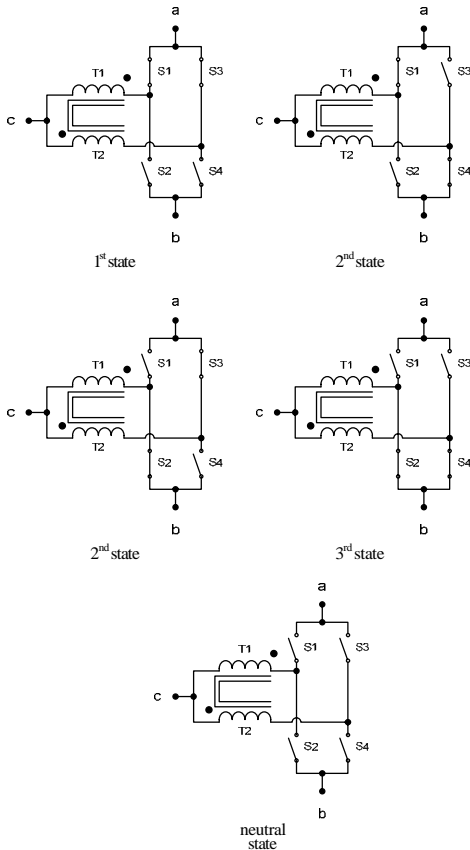


Fig. 4 - Switching states of a three-state commutation cell.

For the first state both of the upper group switches conduct, for the second state one switch of the upper group and one of the lower group conduct, and for the third state, both of the lower group switches conduct.

It can be observed that, for the second state, there are two possibilities: the first, for switch S1 off, and the second, for switch S3 off. However, from an outside view of the cell, there is no difference if either of the above mentioned possibilities is occurring, thus this cell is named the “three-state commutation cell”.

In continuous conduction mode (CCM), this cell operates in 1<sup>st</sup> and 2<sup>nd</sup> states or in 2<sup>nd</sup> and 3<sup>rd</sup> states, since the duty cycle is greater than or less than 0.5, respectively. In the discontinuous conduction mode, besides the states mentioned for CCM, there is also the neutral state.

### B. Drive signals

The switches composing the three-state commutation cell should obey the following drive rule: same-leg switches should be driven in a complementary fashion, whereas different-leg switches should have a 180° lag between their drive signals, that is, half cycle.

The duty cycle is determined by expression (1).

$$D = \frac{t_{onS1}}{T} \quad (1)$$

Where:

- $t_{onS1}$  – conducting interval of switch S1;
- $T$  – switching period.

Converters based on this commutation cell have two operating regions, given as a function of the operational duty cycle, namely: region A, when the duty cycle is less than 0.5; region B, when the duty-cycle is greater than 0.5.

Fig. 5 shows the drive signals of the switches for region A, notice that there is no superposition of the drive signals of switches S1 and S3. On the other hand, Fig. 6 shows the same signals for region B, where the superposition of the drive signals for switches S1 and S3 occur.

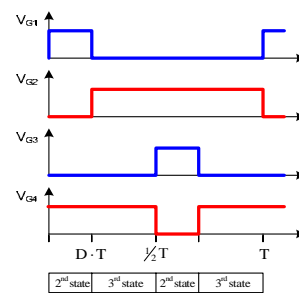


Fig. 5 - Drive signals of the switches for region A ( $D < 0.5$ ).

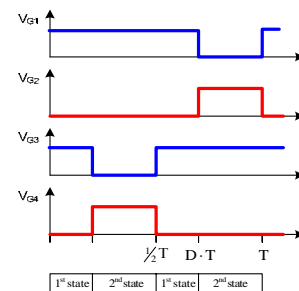


Fig. 6 - Drive signals of the switches for region B ( $D > 0.5$ ).

In both cases the current operating state of the cell is also presented, observe that for region A, the 1<sup>st</sup> and 2<sup>nd</sup> states are present, and for region B, the 2<sup>nd</sup> and 3<sup>rd</sup> states are present.

### III. HALF-BRIDGE CONVERTER

Fig. 7 depicts the power stage of the classic half-bridge converter while Fig. 8 presents the half-bridge converter based on the three-state commutation cell with bidirectional current flow. The only difference that can be observed is the change of commutation cell.

For both operating regions the operation and the main waveforms of the converter will be presented in the following section.

#### A. Operating region $A - D < 0.5$

The operation of the converter in CCM for  $D < 0.5$  is described as follows. Fig. 9 and Fig. 10 depict the operating stages of the converter, while Fig. 11 illustrates its main waveforms.

##### 1<sup>st</sup> Stage ( $t_0 < t < t_1$ )

At the instant  $t_0$  switch S1 starts conducting, and S2 is switched off. Fig. 9a shows this operating stage, where the branches through which the current circulates are in bold; in this stage the commutation cell is in the second state. The simplified circuit of this stage can be observed in Fig. 10a.

Due to the magnetic effect of the transformer, the currents through the transformer windings are identical, thus, the load current is divided, one part through winding T1 and switch S1 and the other through winding T2 and switch S4.

Note that the voltage across winding T2 during this stage is half of the bus voltage. Therefore, the voltage at point A is given by (2) and the voltage imposed across the load during this stage is given by (4).

$$V_a = \frac{1}{2}V_{in} \quad (2)$$

$$V_b = \frac{1}{2}V_{in} \quad (3)$$

$$V_{ab} = \frac{1}{2}V_{in} - \frac{1}{2}V_{in} = 0 \quad (4)$$

##### 2<sup>nd</sup> Stage ( $t_1 < t < t_2$ )

At the instant  $t_1$  switch S1 is turned off, thus switch S2 starts conducting. Fig. 9b shows this operating stage and the simplified circuit is depicted in Fig. 10b. In this stage, it can be observed that the commutation cell is in the 3<sup>rd</sup> state.

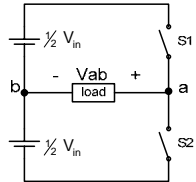


Fig. 7 – Classic half-bridge converter.

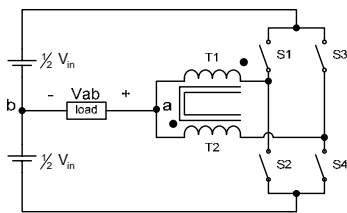


Fig. 8 – Proposed half-bridge converter.

The transformer windings are short-circuited through switches S2 and S4, thus the voltage across the windings is zero. In this stage, the voltage at point A is given by (5), and the voltage across the load is given by (7).

$$V_a = 0 \quad (5)$$

$$V_b = \frac{1}{2}V_{in} \quad (6)$$

$$V_{ab} = 0 - \frac{1}{2}V_{in} = -\frac{1}{2}V_{in} \quad (7)$$

##### 3<sup>rd</sup> Stage ( $t_2 < t < t_3$ )

At the instant  $t_2$ , which is equivalent to half of the switching period, switch S3 starts conducting, and switch S4 is turned off. Fig. 9c shows this operating stage, in which the commutation cell is in the 2<sup>nd</sup> state.

The behavior of the circuit during this stage is similar to the first one, with a single difference regarding the switches that are conducting and, as a consequence, the polarity of the voltage across the transformer.

##### 4<sup>th</sup> Stage ( $t_3 < t < t_4$ )

At the instant  $t_3$  switch S3 is turned off, thus switch S4 starts conducting. Fig. 9d depicts this stage, which is identical to the second one.

This stage ends at instant  $t_4$  when switch S1 starts conducting, thus starting a new switching period.

##### Average load voltage

The average voltage across the load, for a switching period, can be obtained from Fig. 11. Notice that, for this converter, is sufficient to analyze half of the operating period, keeping in mind that regarding the output voltage, the stages repeat themselves every half period, thus the average voltage across the load is given by (10).

$$V_{ab} = \frac{2}{T} \cdot \int_{t_0}^{t_1} 0 \cdot dt + \int_{t_1}^{t_2} -\frac{V_{in}}{2} \cdot dt \quad (8)$$

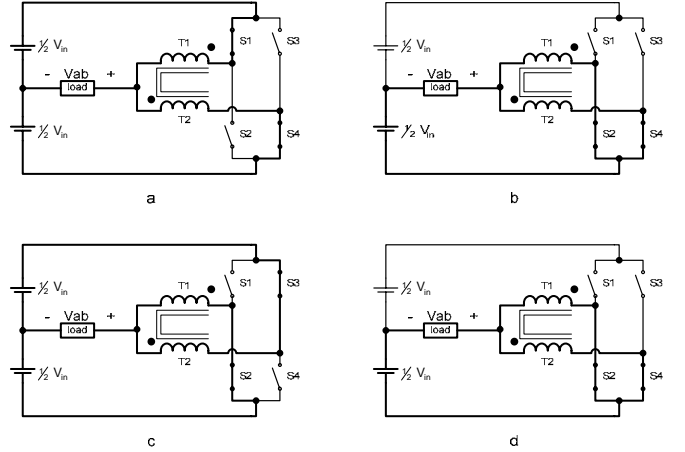


Fig. 9 - Operating stages ( $D < 0.5$ ).

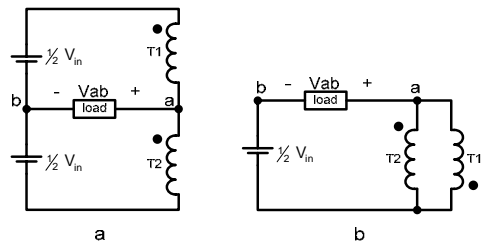


Fig. 10 – Simplified circuits ( $D < 0.5$ ).

$$V_{ab} = \frac{2}{T} \left( -\frac{V_{in}}{2} \cdot (\frac{1}{2} \cdot T - D \cdot T) \right) \quad (9)$$

$$V_{ab} = \frac{V_{in}}{2} \cdot (2D - 1) \quad (10)$$

### B. Operating region $B - D > 0.5$

The operation of the converter in CCM for  $D > 0.5$  is described as follows. Fig. 12 and Fig. 13 depict the operating stages of the converter, while Fig. 14 illustrates its main waveforms.

#### 1<sup>st</sup> Stage ( $t_0 < t < t_1$ )

At the instant  $t_0$  switch S1 starts conducting, and S2 is switched off. Fig. 12a shows this operating stage, where the branches through which the current circulates are in bold; in this stage the commutation cell is in the first state. The simplified circuit of this stage can be observed in Fig. 13a.

The transformer windings are short-circuited through switches S1 and S3, thus the voltage across the windings is zero. In this stage, the voltage at point A is given by (11), and the voltage across the load is given by (13).

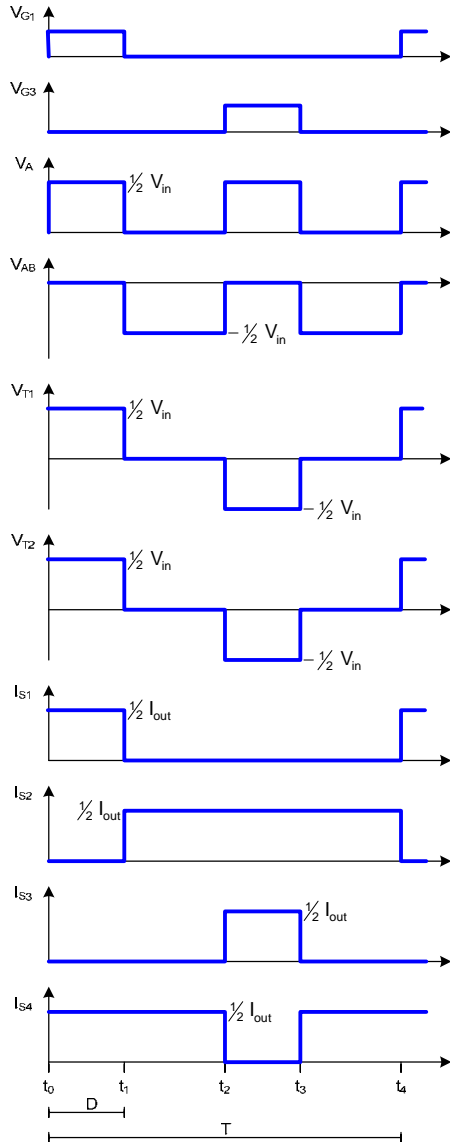


Fig. 11 – Basic waveforms ( $D < 0.5$ ).

$$V_a = V_{in} \quad (11)$$

$$V_b = \frac{1}{2} V_{in} \quad (12)$$

$$V_{ab} = V_{in} - \frac{1}{2} V_{in} = \frac{1}{2} V_{in} \quad (13)$$

#### 2<sup>nd</sup> Stage ( $t_1 < t < t_2$ )

At the instant  $t_1$  switch S3 is turned off, thus switch S4 starts conducting. Fig. 12b shows this operating stage and the simplified circuit is depicted in Fig. 13b. In this stage, it can be observed that the commutation cell is in the 2<sup>nd</sup> state.

Note that the voltage across winding T2 during this stage is half of the bus voltage. Therefore, the voltage at point A is given by (14) and the voltage imposed across the load during this stage is given by (16).

$$V_a = \frac{1}{2} V_{in} \quad (14)$$

$$V_b = \frac{1}{2} V_{in} \quad (15)$$

$$V_{ab} = \frac{1}{2} V_{in} - \frac{1}{2} V_{in} = 0 \quad (16)$$

#### 3<sup>rd</sup> Stage ( $t_2 < t < t_3$ )

At the instant  $t_2$ , which is equivalent to half of the period, switch S3 starts conducting, and switch S4 is turned off. Fig. 12c depicts this stage, which is identical to the first one.

#### 4<sup>th</sup> Stage ( $t_3 < t < t_4$ )

At the instant  $t_3$  switch S1 is turned off, thus switch S2 starts conducting. Fig. 12d shows this operating stage, in which the commutation cell is in the 2<sup>nd</sup> state.

The behavior of the circuit during this stage is similar to the second one, with a single difference regarding the switches that are conducting and the polarity of the voltage across the transformer.

This stage ends at instant  $t_4$  when switch S1 starts conducting, thus starting a new switching period.

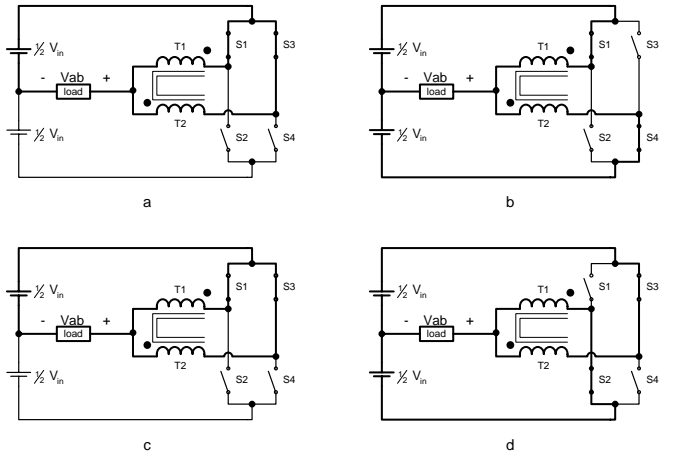


Fig. 12 - Operating stages ( $D > 0.5$ ).

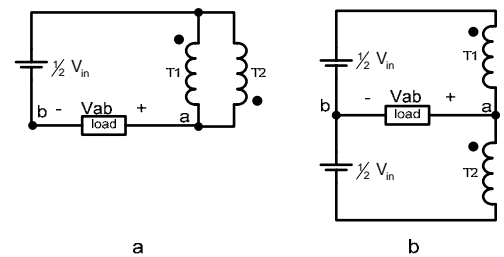


Fig. 13 – Simplified circuits ( $D > 0.5$ ).

### Average load voltage

The average voltage across the load, for a switching period, can be obtained from Fig. 14 and is given by (17). As for region A, it is possible to analyze only half of the switching period, thus the average voltage across the load is given by (19).

$$V_{ab} = \frac{2}{T} \cdot \int_{t_2}^{t_3} \frac{V_{in}}{2} \cdot dt + \int_{t_3}^{t_4} 0 \cdot dt \quad (17)$$

$$V_{ab} = \frac{2}{T} \left( \frac{V_{in}}{2} \cdot (D \cdot T - \frac{1}{2} \cdot T) \right) \quad (18)$$

$$V_{ab} = \frac{V_{in}}{2} \cdot (2D - 1) \quad (19)$$

## IV. OPERATION AS AN INVERTER

For operating region A, negative output voltage values can be obtained, which are bounded by limits  $-V_{in}/2$  and zero. For operating region B, positive output voltage values are obtained within the limits of zero and  $V_{in}/2$ .

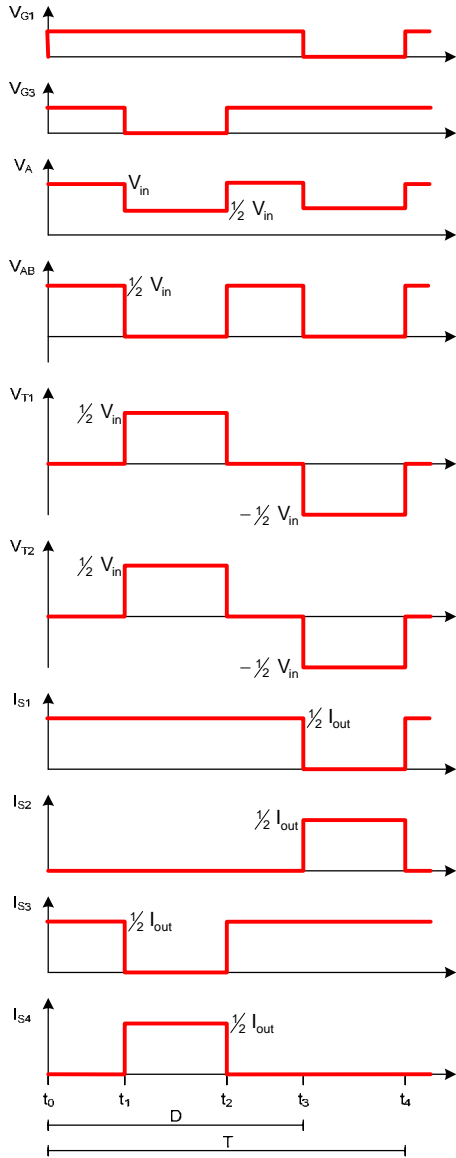


Fig. 14 – Basic waveforms ( $D > 0.5$ ).

It should be stressed that (10) and (19), which determine the average output voltage for both operating regions, are identical and there is no discontinuity when going from one region to the other. Fig. 15 presents the average output voltage for the entire operation range of the converter.

Keeping in mind the limits of the output voltage,  $-V_{in}/2$  and  $V_{in}/2$ , it can be concluded that by using the proper modulation strategy and filtering, a sinusoidal voltage waveform can be obtained at the output of the converter.

### A. Sinusoidal PWM Modulation

The modulation used for the analysis, simulations and implementation of this structure is presented in Fig. 16 and is known as classic sinusoidal PWM. In the implemented circuit, this modulation was made through a DSP.

The drive signal of switch S1 is obtained by comparing the sinusoidal voltage reference ( $V_{sin}$ ) and the triangular voltage waveform ( $V_{tri}$ ). The drive signal of switch S2 is complementary to that of switch S1.

The drive signal of switch S3 has the same duration as the drive signal of switch S1, however, it lags by half of a switching cycle.

## V. STUDY OF THE TRANSFORMER

The high frequency transformer of this structure does not provide isolation, its duties are to divide the current evenly and provide a third voltage level at the output.

Figures 11 and 14 present the voltages across the transformer windings for operating regions A and B, respectively. In both cases the maximum voltage across the windings is half of  $V_{in}$  and the total time the transformer is submitted to this voltage level is a function of the operational duty cycle.

When operating as an inverter, the worst scenario from the standpoint of the voltage across the windings, occurs when the duty cycle is 0.5, as depicted on Fig. 17.

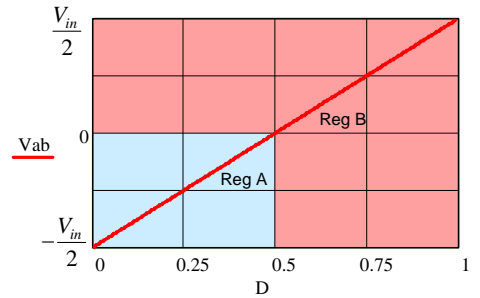


Fig. 15 - Average output voltage.

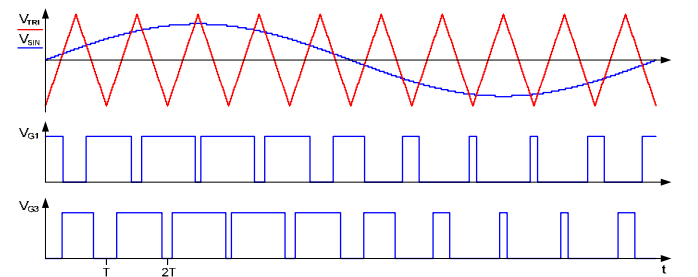


Fig. 16 - Sinusoidal PWM modulation.

When regarding the current through the windings, the current through each of the windings is equal to half of the load current for any duty cycle and for any type of load.

In this manner, with the knowledge of the voltage across and the current through the windings, the transformer can be easily designed.

## VI. STUDY OF THE OUTPUT FILTER

As with classic PWM inverters, this inverter presents an alternating high frequency rectangular voltage on the load terminals, modulated by a low frequency fundamental component. Therefore, it is necessary to include a filter at the output of the inverter, so that a sinusoidal voltage with low harmonic content can be obtained.

Several types of filters can be used for inverters and, in this particular case, a lowpass LC filter was chosen, as illustrated on Fig. 18. Its transfer function of the output voltage with respect to the input voltage is given by (20) [11].

Parameters  $C_f$  and  $L_f$  can be determined by using (21) and (22), taken from [11]. The cutoff frequency ( $f_o$ ) should be at a decade below the frequency of voltage  $V_{ab}$ , that is, it should be at 1/5 of the switching frequency. Also, the damping factor ( $\xi$ ), should not be chosen too small in order to avoid amplifications at the cutoff frequency.

$$\frac{V_{out}}{V_{ab}}(s) = \frac{1}{s^2 L_f C_f + s \frac{L_f}{R_o} + 1} \quad (20)$$

$$C_f = \frac{1}{4\pi \cdot \xi \cdot f_o \cdot R_o} \quad (21)$$

$$L_f = \frac{1}{(2\pi \cdot f_o)^2 \cdot C_f} \quad (22)$$

## VII. SIMULATION RESULTS

The simulation results of the half-bridge inverter using a three-state commutation cell and sinusoidal PWM modulation are presented.

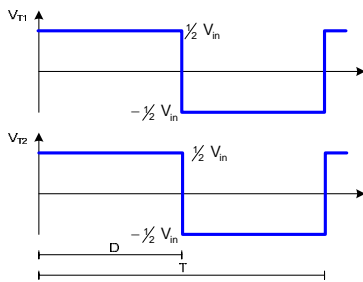


Fig. 17 – Voltages across the transformer windings.

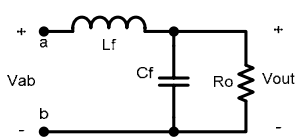


Fig. 18 – Lowpass LC filter.

Fig. 19 depicts the main waveforms of the circuit, which comply with operation principles described earlier. The software used of simulation is the *PSIM Demo Version 6.0*.

Two characteristics of this converter should be emphasized: the frequency at the load is twice the switching frequency and the output voltage has three levels. During the positive semi-cycle the output voltage presents levels 0 and  $V_{in}/2$ , whereas during the negative semi-cycle it presents the levels 0 and  $-V_{in}/2$ . These features minimize the output voltage filtering efforts.

Fig. 20 presents the harmonic spectra of voltage  $V_{ab}$  for the classic half-bridge inverter and for the proposed frequency of 20kHz. It can be observed that the three-level half-bridge converter presents a significant reduction in the harmonic content.

## VIII. EXPERIMENTAL RESULTS

In order to demonstrate the principle of operation and validate the analytical studies presented in this paper, an inverter with the characteristics depicted below was implemented.

- $P_{out} = 1000$  W, output power;
- $V_{out} = 127$  V, output voltage;
- $V_{in} = 450$  V, input voltage;
- $f_s = 24$  kHz, switching frequency;
- $f = 60$  Hz, output frequency;
- $L_f = 500$   $\mu$ H, filter inductor;
- $C_f = 2.2$   $\mu$ F, filter capacitor.

Figure 27 shows the photograph of the prototype implemented.

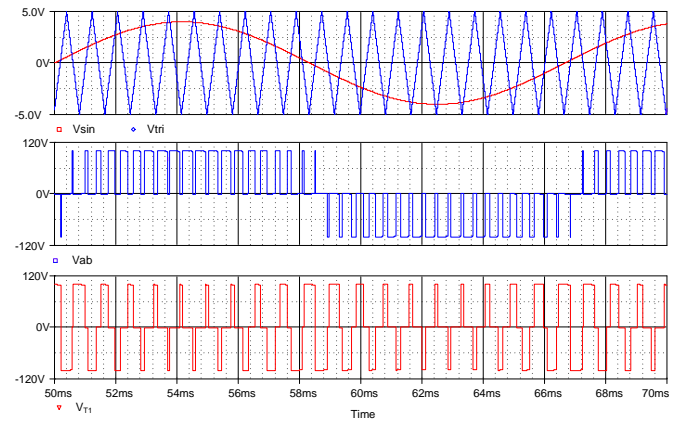


Fig. 19 - Simulation results.

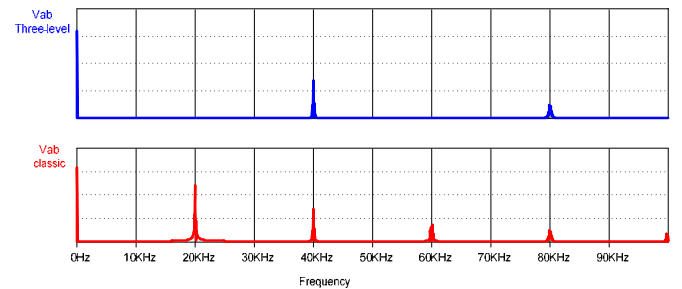


Fig. 20 - Harmonic spectra.

Figure 21 shows the voltage and the current of the load at rated operating conditions. Figure 22 shows the  $V_{ab}$  voltage, output voltage and the current in the filter inductor, it can be noted that the  $V_{ab}$  voltage has three levels.

In Fig. 23 and Fig. 24 the  $V_a$  voltage,  $V_{ab}$  voltage and the current in the filter inductor when the converter operates with a duty-cycle of  $D=0.1$  and  $D=0.9$  are shown, respectively.

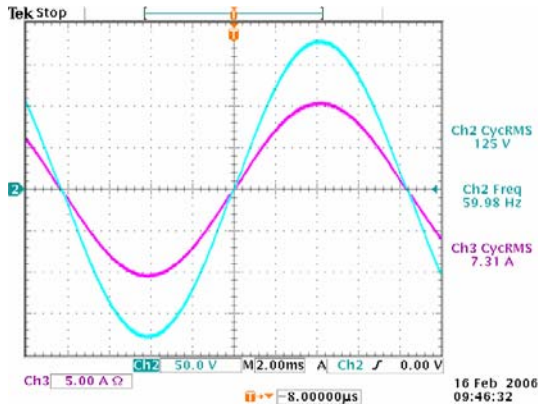


Fig. 21 – Output voltage(Ch2) and output current(Ch3).

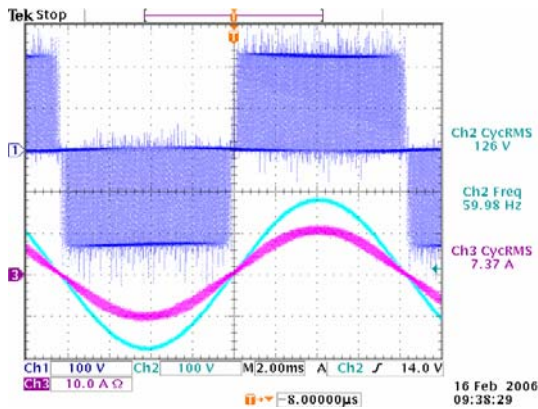


Fig. 22 –  $V_{ab}$  voltage (Ch1), output voltage (Ch2) and Lf current(Ch3).

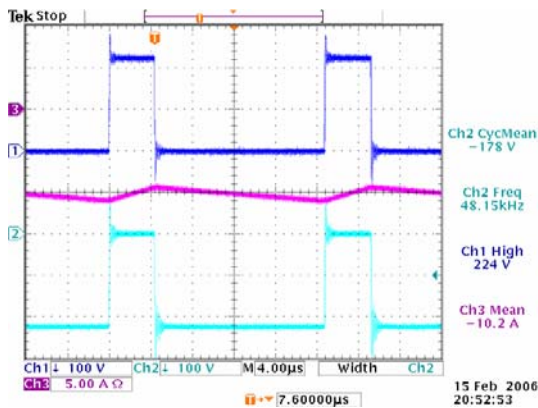


Fig. 23 –  $V_a$  voltage (Ch1),  $V_{ab}$  voltage (Ch2) and Lf current(Ch3) ( $D \cong 0.1$ ).

In Fig. 25 the voltage across the switch S2 and the filter inductor current when the converter operates with a duty-cycle of  $D=0.1$  are shown.

Figure 26 shows the current of the filter inductor and the currents in the windings of transformer. It can be noted that the current in each winding of the transformer is approximately a half of the filter inductor current.

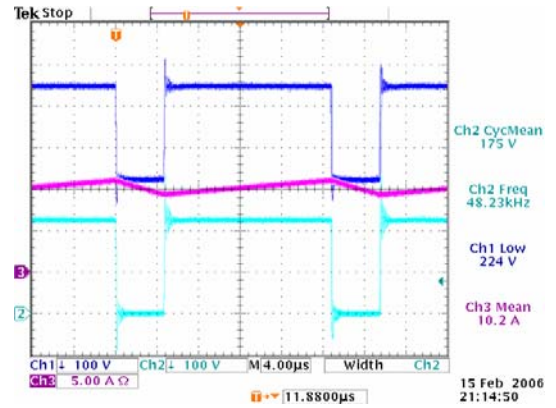


Fig. 24 –  $V_a$  voltage (Ch1),  $V_{ab}$  voltage (Ch2) and Lf current(Ch3) ( $D \cong 0.9$ ).

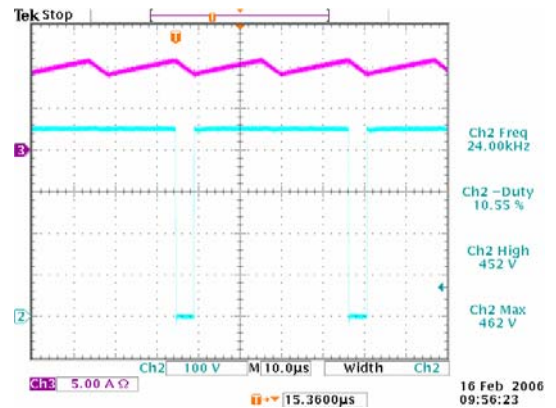


Fig. 25 –  $V_{S2}$  voltage (Ch2) and Lf current(Ch3) ( $D \cong 0.1$ ).

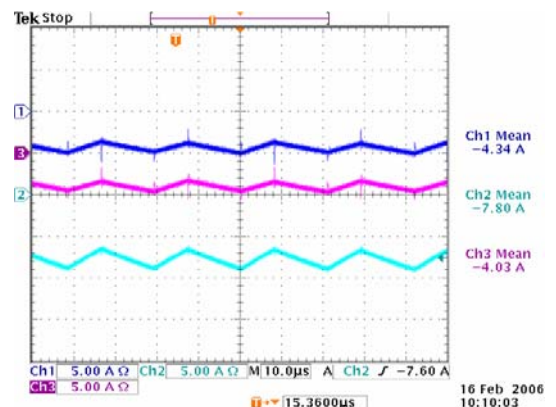


Fig. 26 – Current of windings of the transformer (Ch1 and Ch3) and Lf current(Ch2).

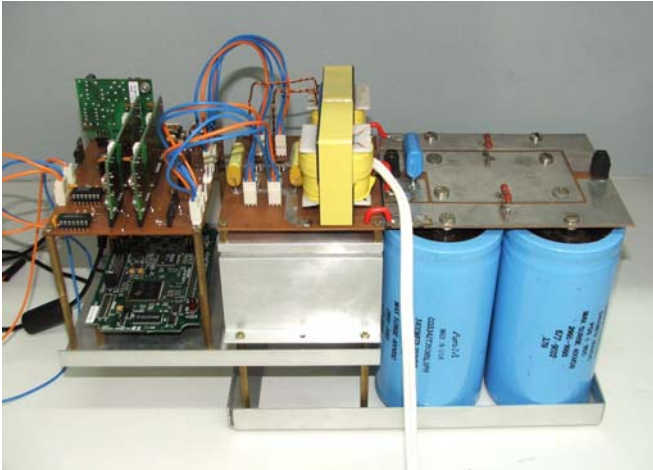


Fig. 27 - Photograph of the prototype.

## IX. CONCLUSIONS

In this paper, a new three-level half-bridge inverter, which uses a three-state commutation cell, was proposed. For this converter, the operation principles, as well as simulation and experimental results were presented.

Among the advantages of the three-level half-bridge inverter, it is worth emphasizing: the output voltage presents three levels and its frequency is twice the switching frequency, making filtering an easier task; the current is divided amongst the switches, therefore, reducing the conduction losses.

The disadvantages are the need for a transformer as well as a higher number of switches.

In light of its characteristics and the good experimental results obtained, we believe that inverter is appropriate for industrial applications.

The concept of the proposed inverter can be extended to larger number of levels [5,7], and this will be analyzed in future publications.

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