

# A Three-Phase Buck Rectifier with High-Frequency Isolation by Single-Stage

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**Abstract**—In this paper the design and experimental results for the isolate unidirectional three-phase buck rectifier are presented. In the previous work this topology was introduced which utilizes a forward/flyback transformer to allow the high-frequency isolation to a three-phase Buck rectifier without additional power switches. In order to complement the previously acquired knowledge a review of operation states and modulation, power circuit design and discrete control applied to a prototype are described. Such as, the experimental results to  $220V_{rms}$  mains and  $2.5kW$  at  $48V$  load with discrete control and unit power factor is presented.

**Keywords** - three-phase PWM buck rectifier, high-frequency isolation, *dqo* transform.

## I. INTRODUCTION

Some power applications which use three-phase PWM rectifiers the electric isolation between the mains and load is required. In such cases, usually a two-stage power processing unit is used being composed of: a front-end six-switch buck or boost rectifier cascaded with an isolated dc/dc converter. In three-phase uninterruptible power supplies (UPS), isolation is often provided by a bulky commercial frequency transformer either at the ac input or at the dc output side.

The first one high-frequency isolated topology was proposed on the fundamental article [2] using a switch-mode rectifier(SMR) structure that has six hard switching thyristors with bidirectional current flow. An improvement on this topology [3] can be achieved by using the PWM control method for the SMR, based on coordinate transforms. In this method the iron loss in the transformer may become visible because of the high-frequency.

Reference [4] proposed a novel ZVS PWM three-phase rectifier, topologically equivalent to the converter described in [2] and [3] but potentially is improved by a ZVS strategy which makes use of the parasitic capacitances of the switches and the transformer leakage inductance. However, to obtain all the benefits of this structure, twelve power switches (MOSFETs or IGBTs) and a sophisticated PWM strategy are required for effective implementation.

The paper presents design specifications supplementaries to the original paper [1] which the novel topology of single stage isolated three-phase rectifier was introduced. The implemented power circuit is depicted in Fig. 1 and prototype design with relevant equations transformer and the others circuits for a set given design specifications are presented. The topology is

proved by experimental results from  $2.5kW$  at  $48V$  micro-processor controlled prototype.

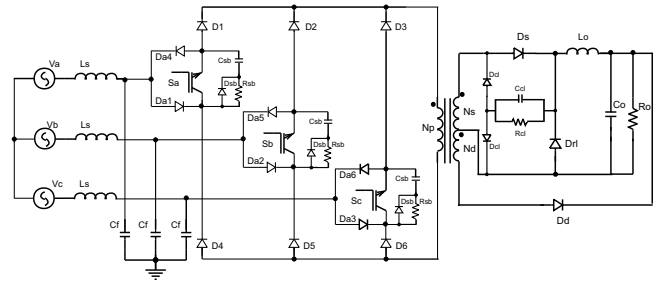


Fig. 1. Three-Phase Buck Rectifier with High-Frequency Isolation by Single-Stage. (PCT/BR2007/000084)

## II. FORWARD/FLYBACK CONVERTER

The high-frequency isolation is achieved by a forward/flyback converter [5], which operates as forward converter with transformer demagnetization through the load. It is composed by a forward sub-converter operates in continuous conduction mode (CCM) and the flyback sub-converter in discontinuous conduction mode (DCM). Hence, the forward sub-converter processes almost all power delivered to the load. The Fig. 2 shows the topology of the forward/flyback converter.

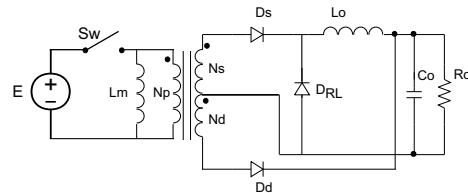


Fig. 2. Forward/flyback converter.

From the *volt · second* balance, the ratio of the demagnetizing turns per primary turns is obtained which, ensures the demagnetization of the transformer's core and operation of the flyback sub-converter in DCM.

$$\frac{N_d}{N_p} \leq \frac{V_o}{E} \cdot \frac{(1-D)}{D} \quad (1)$$

### III. OPERATION STATES

The operation states to a sextant of mains angular period is commented in this section. At each sextant 4 states can be always identified, in following figures the considered sextant is between  $0^\circ$  and  $60^\circ$  with states 1, 2 and 0 involved.

Fig.3 the switches S2 and S3 are enable and the energy is transfer through transformer to load by Ds diode. Fig.4 the switches S1 and S2 are enable and the energy transfer through transformer to load is continued by Ds diode.

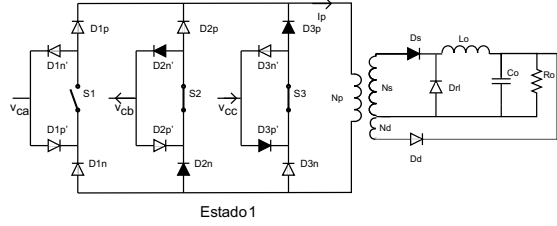


Fig. 3. First state.

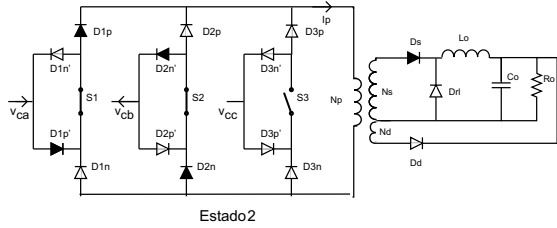


Fig. 4. Second state.

When the switches on the rectifier bridge are disenable the magnetization is extinct by Dd diode through the load in Fig.5. In order to assure a complete demagnetization a dead time is provided by a free-wheel current circulation in the end of 0 state, see Fig.6.

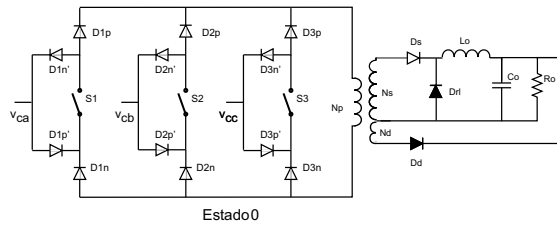


Fig. 5. Demagnetization state.

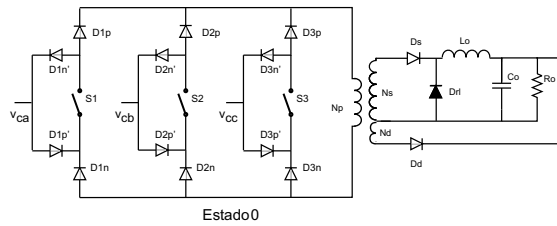


Fig. 6. Free-wheel state.

### IV. PROTOTYPE DESIGN AND IMPLEMENTATION

In order to demonstrate the feasibility for the topology an experimental prototype was designed according the project set:  $V_{line-line} = 220V$ ;  $f_s = 30kHz$ ;  $P_o = 2.5kW$ ;  $V_o = 48V$ .

#### A. Input Filter Design

An appropriate design of the AC input filter was carried out to provide a high power-factor, and T.H.D of line current intending to complain with IEC 61000-3-2 A Class, it was employed a classical low-pass LC filter which has a capacitance value defined according to the equation below:

$$C_f \leq \frac{2 \cdot P_o}{3 \cdot \eta \cdot \omega \cdot V_{cf}^2} \cdot \tan(\cos^{-1}(\phi)) = 25\mu F \quad (2)$$

The presented parameters at equation 2 are defined as follow:  $V_{cf} = 180V$  peak input filter capacitor voltage;  $\eta = 0.8$  estimated overall efficiency;  $\phi = 0,99$  estimated displacement factor and  $\omega = 2 \cdot \pi \cdot f$  line frequency. It was decided by an Epcos polypropylene power capacitor  $C_f = 22\mu F$  and defined a cut frequency for the input filter at  $280Hz$  results an input filter inductance  $L_s = 190\mu H$ .

#### B. Transformer Design

The design procedure is based on usual equations to design E core high-frequency transformers where it was defined by following constrains parameters:  $\Delta B = 0.18Tesla$  variation flux density ;  $J = 450 \frac{A}{cm^2}$  current density;  $k_p = 0.7$  winding fill factor;  $k_w = 0.4$  spool factor.

$$AeAw = \frac{2 \cdot P_o \cdot 10^4}{k_p \cdot k_w \cdot J \cdot f_s \cdot \Delta B \cdot \eta} = 98cm^4 \quad (3)$$

It was selected a core E75/IP12 which were associated three cores in order to exceed the calculated  $AeAw$  at equation 3 where it was obtained a  $AeAw = 125cm^4$  and a total cross-sectional area  $Ae = 19.35cm^2$ .

The number of turns to each transformer winding are defined by the following equations where  $V_{ret,max} = 311V$  maximum rectified voltage;  $V_{ret,min} = 290V$  minimum rectified voltage;  $D_M = 0.5$  maximum duty cycle and  $D = 0.3$  average duty cycle:

$$N_p = \frac{V_{ret,min} \cdot 10^4}{2 \cdot Ae \cdot \Delta B \cdot f_s} = 14turns \quad (4)$$

$$N_s = 1.1 \cdot \frac{N_p \cdot (V_o + 1.5 \cdot D)}{D \cdot V_{ret,min}} = 9turns \quad (5)$$

$$N_d = N_p \cdot \frac{V_o}{V_{ret,max}} \cdot \frac{(1 - D_M)}{D_M} = 2turns \quad (6)$$

### C. Rectifier Bridge Design

The Buck rectifier operates at forced-commutation, therefore to power switches and diodes bridge more careful consideration has to be given to choice these devices.

The *RCD* snubbers were associated to the power switches to control the voltage rise rate reducing the stress and power dissipation in switch at turn-off, the Fig.1 presents the snubbers and switches association. For this design, 600V 55A IGBT's were selected.

For this design the peak switch voltage unless turn-off is:

$$V_{swpk} = \begin{cases} \frac{N_p}{N_d} \cdot V_o & \text{for } \frac{N_p}{N_d} \cdot V_o > \sqrt{2} \cdot V_{line} \\ \sqrt{2} \cdot V_{line} & \text{for } \frac{N_p}{N_d} \cdot V_o \leq \sqrt{2} \cdot V_{line} \end{cases}$$

### D. Output Design

The output design regards the secondary diodes,  $D_s$ ,  $D_{RL}$ ,  $D_d$ , and output filter *LC*. The diodes  $D_s$  and  $D_{RL}$  were preserved by voltage clamping illustrated in Fig.1. For this design, 400V 115A Ultrafast rectifier diodes were selected to  $D_s$  and  $D_{RL}$  and a *RCD* clamp with resistance of  $5.8k\Omega$  and a capacitance of  $150nF$  was applied. The output filter is composed by 100V electrolytic capacitors in parallel with total capacitance of  $4400\mu F$  and the inductors were designed for a total inductance of  $600\mu H$  composed by two toroidal core inductors of  $300\mu H$ .

### E. Controller Board Design

The conditioning signal circuits, 2.5V offset circuits and adder circuits were designed to operational amplifier OPA2222. The sampled currents and voltages are processed for dsPIC30F4011, with 16 bit digital signal microcontroller, 10 bit AD converters and up to 30MIPS instruction processing.

The sampling frequency is 15kHz with a PWM frequency into *dsPIC* of 15kHz. At first stage of signal conditioning it was designed an anti-aliasing filter with characteristic frequency of 2.5kHz. In order to eliminate the negative values of sampled line current it was designed a non-inverter adder for 2.5V offset.

The three-level modulation was implemented through a XOR TTL integrated circuit in order to improve the processing time on *dsPIC* and this PWM is used as input signal to commercial IGBT's drives.

The block diagram depicted in Fig. 7 comprises the isolated buck rectifier and the main blocks to the discrete control implementation based on dsPIC microcontroller technology.

The picture Fig.8 illustrates the prototype, where in the left are the AC input filter, inductors and film power capacitors, in the middle is the Buck rectifier bridge, in the right the transformer and the output filter. Attached to front of prototype is the conditioning, processing and controller board.

## V. DESIGN OF DISCRETE CONTROL

The AC and DC models were obtained based on phase variables in the *dqo* coordinates system according the previous

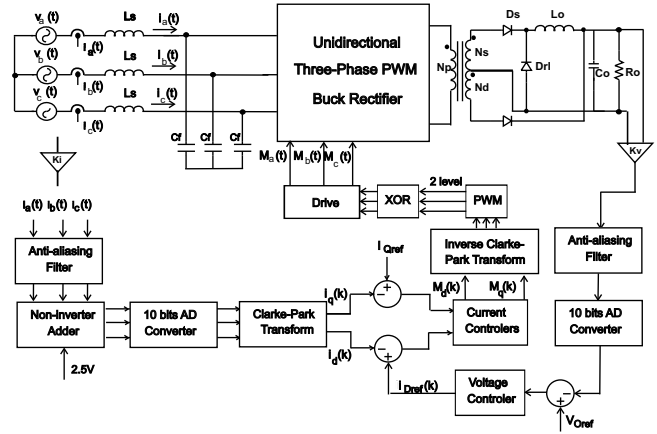


Fig. 7. Discrete control loop block diagram.

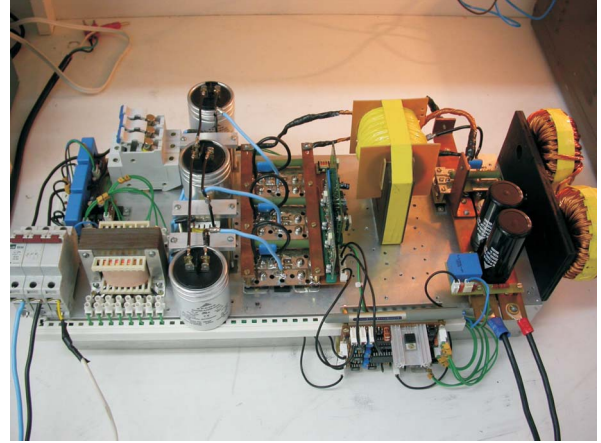


Fig. 8. Implemented experimental prototype.

article [1]. The both models present a second-order characteristics for the AC input currents,  $G_i(z)$ , and the DC load voltage,  $G_v(z)$ , as represented by the discrete transfer functions below:

$$G_i(z) \Leftarrow ZOH(s) \cdot G_i(s) \quad (7)$$

$$G_i(z) = 7,38 \cdot \frac{(z + 2,39) \cdot (z + 0,156)}{(z - 0,12) \cdot (z^2 - 1,01z + 0,96)} \quad (8)$$

$$G_v(z) \Leftarrow ZOH(s) \cdot G_v(s) \quad (9)$$

$$G_v(z) = 0,03 \cdot \frac{(z^2 - 1,01z + 0,84)}{(z - 0,12) \cdot (z^2 - 1,97z + 0,98)} \quad (10)$$

The closed-loop uses *PI* discrete controller, which were designed to control the rectifier by the load voltage and the input currents and them implementation at assembly code obtained through *deference equations*. Such as, the designed discrete transfer function for the current controller,  $C_i(z)$ , and voltage controller,  $C_v(z)$  are specified by:

$$C_i(z) = 0,000436 \cdot \frac{z - 0,178}{z - 1} \quad (11)$$

$$C_v(z) = 0,0276 \cdot \frac{z - 0,983}{z - 1} \quad (12)$$

## VI. EXPERIMENTAL RESULTS

Operation and performance of designed prototype are illustrated by the following experimental results obtained at load resistance of  $0.89\Omega$  exceeding the designed power of  $2.5kW$ .

The Fig.9 shows an input reference phase voltage and input current, which is perceived the quality for the input current in phase with the voltage. Fig.10 shows the three-phase input currents where phase  $a$  presents low distortion, phase  $b$  and  $c$  are almost sinusoidal. The input capacitor voltage and current are illustrated at Fig.11 where the current carries the high frequency harmonics generated by PWM Buck rectifier bridge with relevant peak current that shall be consider when chosen the capacitor.

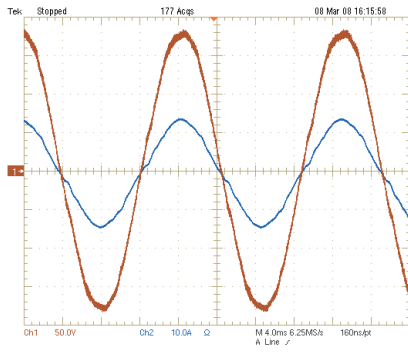


Fig. 9. Phase voltage and current.

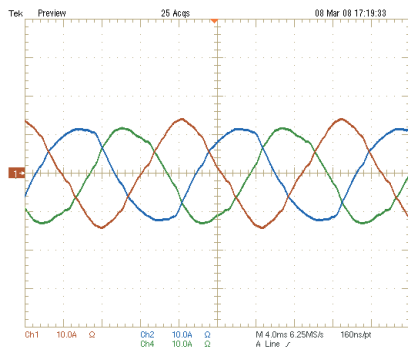


Fig. 10. Input currents.

Fig.12 shows the voltage and current in a power switch, upper is a view at low frequency and below is the expanded view with voltage and current follow the safety and expected behavior performed by the snubber assistance. Fig.13 shows the secondary winding voltage and current as well as the demagnetization current. Fig.14 shows the load voltage and current at steady state and the Fig.15 shows the soft-start achieved without auxiliary circuits for the prototype. The power quality is proved in the Fig.16 with a total harmonic distortion of  $6.4\%$  and power factor of  $0.998$  both to phase  $a$ . Fig.17 shows the estimated prototype efficiency at bold line

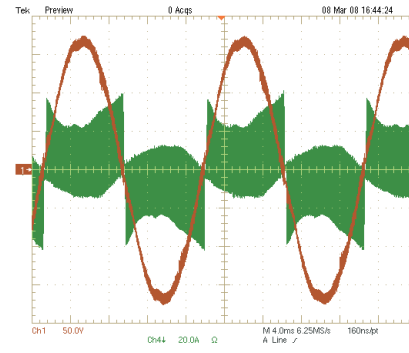


Fig. 11. Input capacitor voltage and current.

and the measured efficiency at four different values of load resistance at dotted line. The overall efficiency at full load is around  $80\%$ .

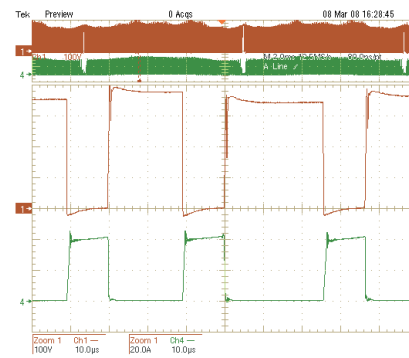


Fig. 12. Switch voltage and current.

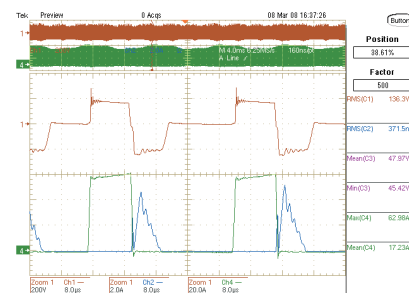


Fig. 13. Secondary voltage and current.

## VII. CONCLUSION

A prototype design, operation and performance of a three-phase Buck rectifier with high-frequency isolation by single-stage was presented and demonstrates the concepts introduced at original work [1].

The topology operates at forced-commutation and achieved a reasonable  $80\%$  overall efficiency at full load although considering the dissipated power at snubbers and clamp circuits. Otherwise, comparing within others isolated topologies this requires three power switches and twelve diodes into rectifier instead of ten or twelve power switches and fast diodes. Such

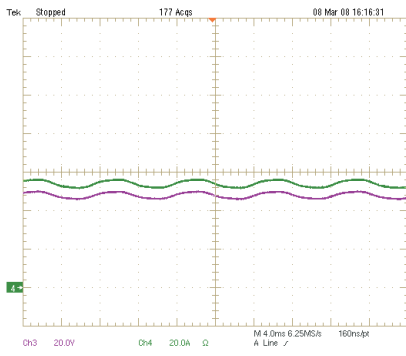


Fig. 14. Load voltage and current.

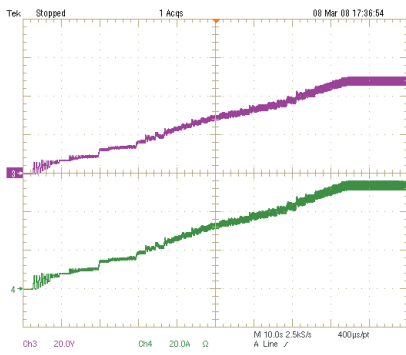


Fig. 15. Load voltage and current at start.

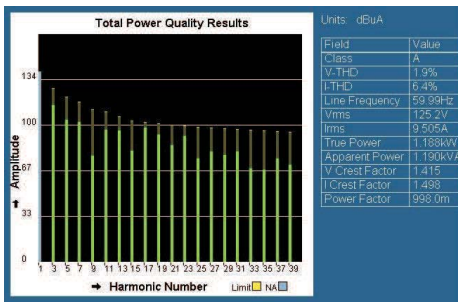


Fig. 16. Power quality analysis.

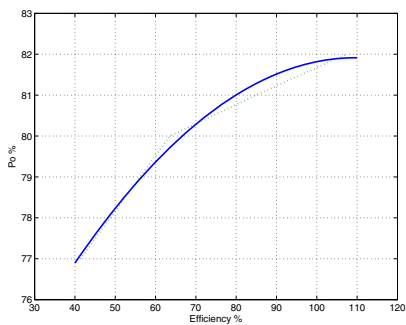


Fig. 17. Prototype efficiency as function of %load power.

as the efficiency curve demonstrates values at light load near to full load presents an almost linear operation.

Concisely being a buck or a forward converter an special

attention should be taken regarding the comprise of voltage and current ratings as well as commutation frequency to a safety operation, i.e. these will be determinant to the rectifiers design and pretense application.

Therefore, this isolated single stage rectifier is a alternative solution for medium-power and high input voltage applications, e.g. telecommunication power supplies or UPS systems which would uses boost rectifiers with high-frequency isolation by additional stage.

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