

A New ZCS Quasi-Resonant Unity Power Factor Rectifier with Reduced Conduction Losses

Alexandre Ferrari de Souza and Ivo Barbi

Federal University of Santa Catarina
Dept. of Electrical Engineering
Power Electronics Institute

P.O. BOX 5119 - 88040-970 - Florianópolis - SC - Brazil
Phone : 55-48-231.9204 - Fax : 55-48-231.9770 - e-mail : ivo@lamep.ufsc.br

Abstract - This paper presents a novel single-phase unity power factor rectifier, which features Current-Sense Frequency Control and Zero-Current Switching with no auxiliary switches. The reduced conduction losses are achieved by the employment of a single converter, instead of the typical configuration composed by a front end rectifier followed by a boost converter. Experimental results of a 250 W converter with 127 V_{rms} input voltage and 200 V_{DC} output voltage are presented. Theoretical analysis, a design example, simulation results and the control circuitry are also presented in the paper. The Zero-Current-Switching makes this topology very attractive to high power IGBT applications.

I. INTRODUCTION

The conventional input stage for single phase power supplies operates by rectifying the AC line voltage and filtering with large electrolytic capacitors. This process generates a distorted input current waveform with large harmonic content. Thus, the resulting power factor is very poor (around 0.6). The reduction of input current harmonics and high power factor operation is an important requirement for power supplies, specially when the forthcoming harmonic standards, such as IEC-555-2, must be satisfied. In these applications, AC-DC converters featuring almost unity power factor are required.

The topology usually employed in power factor correction single-phase power supplies is composed by a front end rectifier followed by a boost converter, as shown in Fig. 1.(a). However, this converter presents commutation and conduction losses, which contribute for a reduction on the efficiency. The commutation losses occurs due to the hard switching of power semiconductors and the conduction losses are representative because there are always three semiconductors in the current flow path.

The reduction of the commutation losses can be achieved by different techniques. The circuits presented in references [1] and [2] propose similar techniques using auxiliary commutation circuits, shown in Fig. 1.(b). The efficiency in these converters is improved. However, the conduction losses are still present.

The circuit proposed by reference [3] achieves the soft-switching through a ZCS quasi-resonant technique without any auxiliary switches, as shown in Fig. 1.(c). The efficiency in this converter is also improved, but the conduction losses are still considerable.

The converter presented in reference [4] and shown in Fig. 1.(d) operates with much lower conduction losses than the previous ones. This occurs because the current always flows through two semiconductors simultaneously, instead of three. However, the commutation losses problem is not solved.

In order to improve the efficiency even more and reduce the heat sink size, reference [5] proposed a power factor correction rectifier with soft-commutation and reduced conduction losses, shown in Fig. 1.(e). However, the soft-switching is achieved by an auxiliary commutation circuit with an auxiliary switch.

The purpose of this paper is to present and analyze a new converter, which operates with reduced conduction losses and soft-commutation without any auxiliary switches.

II. THE NEW TOPOLOGY AND PRINCIPLE OF OPERATION

A. Principle of Operation

The power stage diagram of the proposed ZCS high power factor converter is shown in Fig. 2. The operation of the circuit is described as follows. When the input current is positive, the diode D₂ will conduct, while switch S₁ and diode D₃ will perform the boost function with power factor correction. When the input current is in the reverse direction, switch S₂ and diode D₄ will perform the boost function with power factor correction, while diode D₁ will conduct. The resonant components L_{r1}, L_{r2}, C_{r1} and C_{r2} will be responsible for the Zero-Current-Switching of S₁ and S₂.

It can be noticed that in this topology there is no auxiliary switch to perform the soft switching. The topology presents the following characteristics:

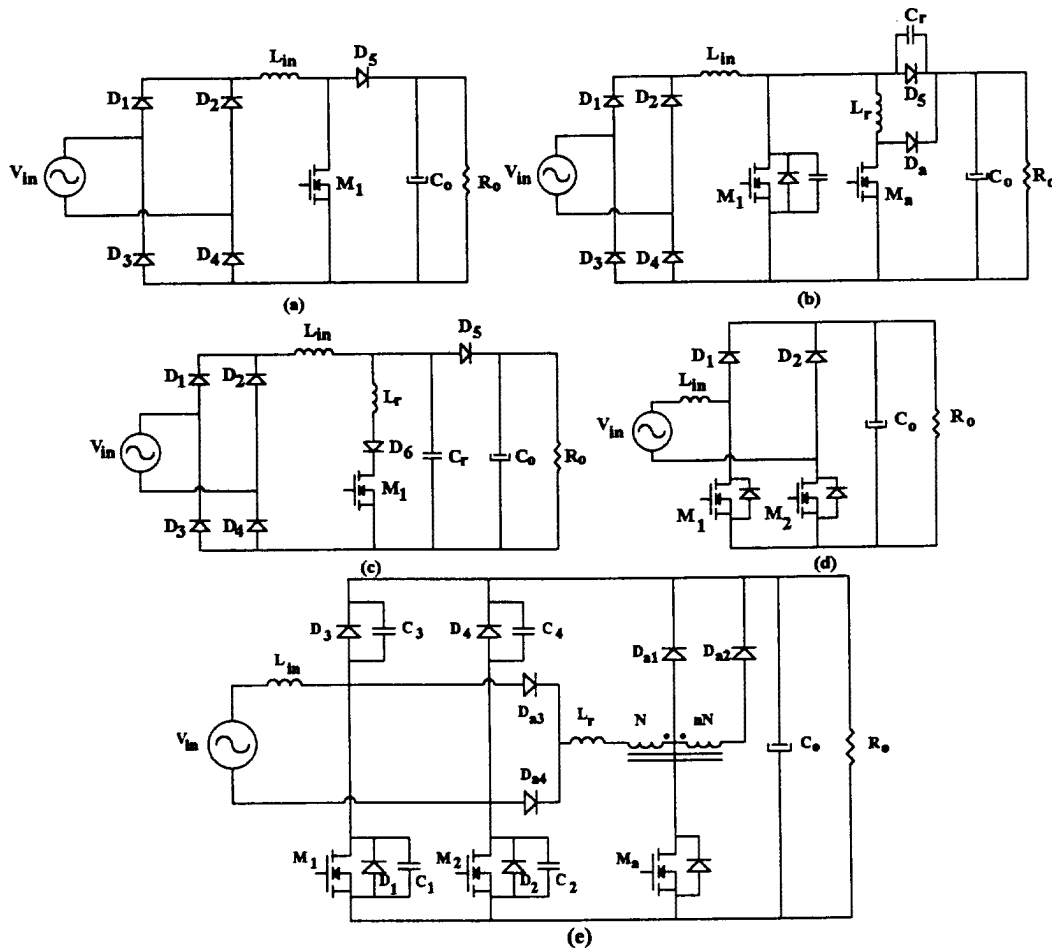


Fig. 1 - Power factor correction topologies presented in references [1], [2], [3], [4] and [5].

- The absence of auxiliary switches to perform the soft-commutation;
- reduced conduction losses, once there are always only two semiconductors in the current flow path;
- capability to draw a sinusoidal input current with the appropriate control;
- better performance of input inductor (L_{in}), once it is located in the AC side.

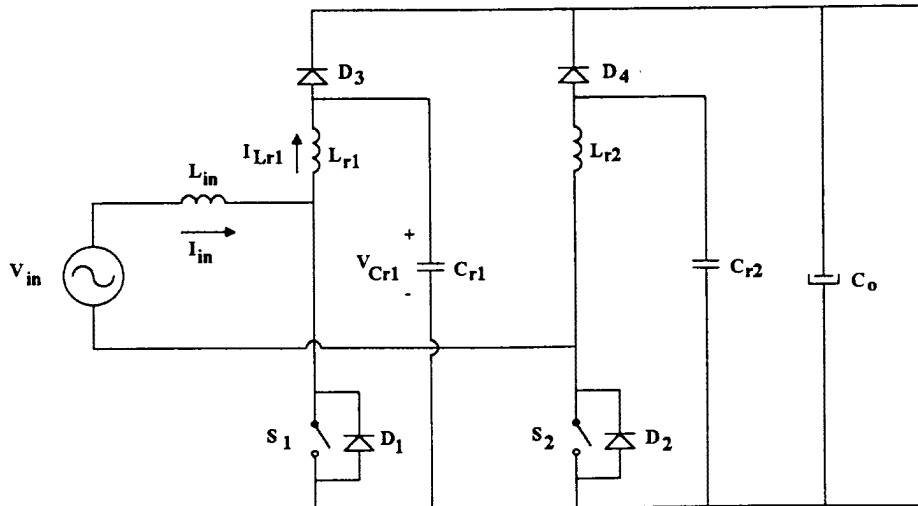


Fig. 2 - ZCS high power factor rectifier with reduced conduction losses.

B. Soft-Commutation Description

The ZCS commutation will occur during a small time when compared to the input voltage oscillation period. Thus, the input voltage can be considered a constant voltage source. In order to analyze the ZCS commutation of the switches S_1 and S_2 , let us assume that a positive current is flowing through L_m , the output voltage V_o is constant and all the components are ideal. Therefore, the topology can be simplified for the analysis of the stages of operation shown in Fig. 3

• **First Stage (t_0, t_1) (Fig. 3.a) - Linear stage.**

At the beginning of this stage the input current was flowing through L_{r1} and D_3 to the output. The capacitor C_{r1} is charged and its voltage is equal to the output voltage. At instant t_1 switch S_1 is turned on under ZCS. The current through S_1 will increase linearly, while the current through L_{r1} will decrease at the same rate. This stage finishes when $I_{Lr1}=0$. At this moment diode D_3 will turn off.

• **Second Stage (t_1, t_2) (Fig. 3.b) - Resonant stage.**

At time $t=t_1$ the current through L_{r1} becomes null and the current through S_1 is equal to the input current. A resonant stage comprising L_{r1} and C_{r1} begins. The current through L_{r1}

begins to decrease in a resonant way, becomes negative, and increases again. The capacitor C_{r1} begins to discharge at the same manner and its voltage becomes negative. At the end of this stage the current through L_{r1} is equal to the input current I_m and the current through S_1 becomes null. The voltage at capacitor C_{r1} is negative.

• **Third Stage (t_2, t_3) (Fig. 3.c) - Resonant stage.**

At time $t=t_2$ diode D_1 is turned on. The resonant current I_{Lr1} increases in a resonant manner, reaches its maximum value and decreases until it is equal to the input current again. The capacitor C_{r1} will be charged and its voltage will become positive. This stage finishes when the current through L_{r1} is equal to the input current. At this moment the diode D_1 is turned off. During this stage the switch S_1 can be turned off under Zero Current Switching.

• **Fourth Stage (t_3, t_4) (Fig. 3.d) - Linear stage.**

When I_{Lr1} becomes equal to I_{in} , capacitor C_{r1} is charged linearly by I_m . This stage finishes when $V_{Cr1}=V_o$. At this moment diode D_3 is turned on.

• **Fifth Stage (t_4, t_5) (Fig. 3.e) - Power transfer stage.**

During this stage, power is transferred from the input (I_m) to the load through diode D_3 .

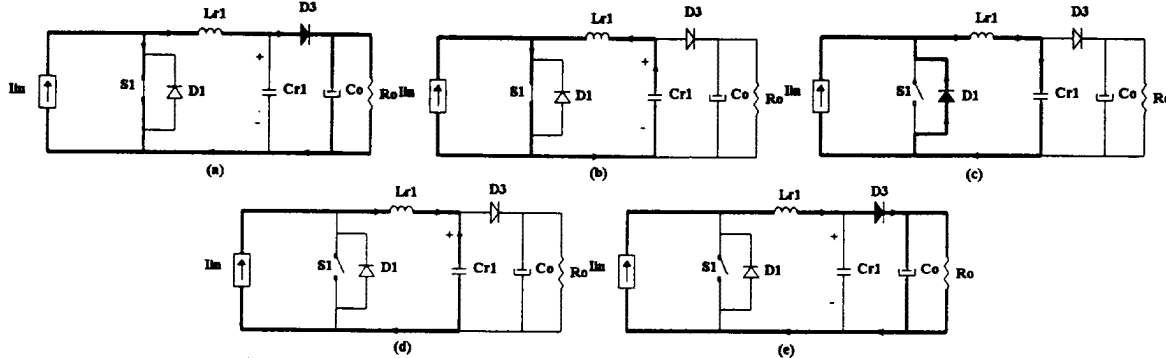


Fig. 3 - Topological stages of the commutation for the simplified ZCS boost converter.

The theoretical waveforms for these five stages are shown in Fig. 4. It can be observed the soft-switching characteristics of this circuit. It is important to notice that the voltage across S_1 is clamped to the output voltage, with no stress. However, due to the resonant characteristics, S_1 presents current stress.

In order to achieve soft-switching the following constraint must be satisfied:

$$\alpha \leq 1 \quad (1)$$

Where:

$$\alpha = \frac{Z_n \cdot I_{in}}{V_o} \quad (2) \quad Z_n = \sqrt{\frac{L_{r1}}{C_{r1}}} \quad (3)$$

The on-time of switch S_1 combined with its anti-parallel diode is defined by expression (4).

$$t_{on} = \Delta t_1 + \Delta t_2 + \Delta t_3 \quad (4)$$

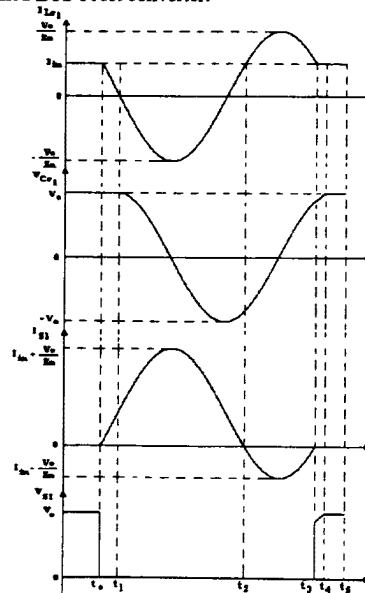


Fig. 4 - Main waveforms for the simplified ZCS boost converter.

III. CONTROL STRATEGY

In order to achieve a high power factor, an appropriated control technique must be employed. The diagram of the control strategy is shown in Fig. 5.

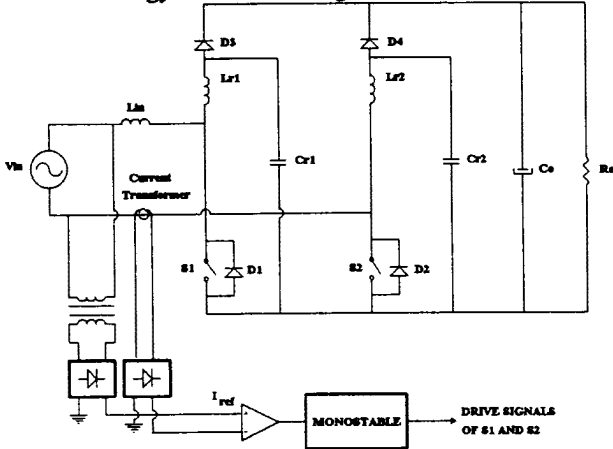


Fig. 5 - Diagram of the employed control strategy.

This technique consists in comparing the input current I_{in} with a sinusoidal reference proportional to the line voltage during the time in which switch S_1 (during positive half-cycle of input voltage) or S_2 (during negative half-cycle of input voltage) is off.

When $I_{in} = I_{ref}$, the corresponding switch S_1 or S_2 is turned on. The switch will remain in this state during a fixed time, provided by a monostable circuit. The waveforms of the control strategy are shown in Fig. 6.

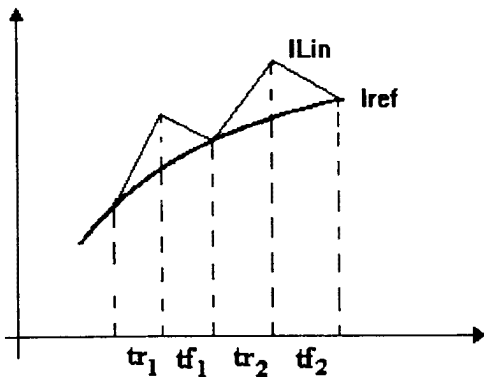


Fig. 6 - Waveforms of the control strategy.

This on-time must ensure the soft-switching of the corresponding switch. Thus the minimum on-time is defined by expression (5)

$$t_{onmin} = \Delta t_1 + \Delta t_2 = \frac{1}{\omega_o} \cdot \{ \alpha(t) + \pi + \sin^{-1}(\alpha(t)) \} \quad (5)$$

Where:

$$\omega_o = \frac{1}{\sqrt{L_{r1} \cdot C_{r1}}} \quad (\text{resonant frequency}) \quad (6)$$

This time will vary along with the instantaneous input current. Thus the $\alpha(t)$ parameter will vary according to the following expression:

$$\alpha(t) = \alpha \cdot \sin(\omega t) = \frac{Z_n \cdot I_{in}}{V_o} \cdot \sin(\omega t) \quad (7)$$

Where : ω = frequency of the input voltage (rad/sec)

Therefore, the minimum on time will occur when the input voltage is zero.

$$t_{onmin} = \frac{\pi}{\omega_o} \quad (8)$$

The maximum on-time is defined by expression (9)

$$t_{onmax} = \Delta t_1 + \Delta t_2 + \Delta t_3 = \frac{1}{\omega_o} \{ \alpha(t) + 2\pi - \sin(\alpha(t)) \} \quad (9)$$

Therefore, the maximum admissible on-time to achieve ZCS will be defined when the input voltage is maximum. Thus:

$$t_{onmax} = \frac{1}{\omega_o} \{ \alpha + 2\pi - \sin \alpha \} \quad (10)$$

According to the expressions (8) and (9) it is possible to determine the on-time provided by the monostable circuit. The rise and fall time of the input current, shown in Fig. 6 are defined by expressions (11) and (12), respectively. The switching frequency will be given by expression (13).

$$t_{fn} = \frac{1}{\omega_o} \left\{ \alpha(t) + 2\pi - \sin^{-1}(\alpha(t)) + \frac{1 - \sqrt{1 - \alpha^2}}{\alpha} \right\} \quad (11)$$

$$t_{fn} = \frac{t_{rn} \cdot \sin(\omega t)}{V_o / V_p - \sin(\omega t)} \quad (12)$$

$$f_{sn} = \frac{1}{t_{rn} + t_{fn}} \quad (13)$$

The converter will operate in continuous current mode with variable switching frequency.

IV. SIMPLIFIED DESIGN PROCEDURE AND EXAMPLE

A. Design Procedure

A simplified design procedure is described in this section as follows:

1. Input Data

- V_o - Output Voltage
- V_p - Peak input Voltage
- P_o - Output Power
- f_o - resonant frequency
- ΔI_{max} - Maximum ripple in the input current

2. Determination of the parameter α_{max}

As already stated, this parameter must be less or equal to unity in order to ensure Zero-Current-Switching.

$$\alpha = \frac{\sqrt{L_{r1} \cdot I_{\min}}}{V_o} \leq 1 \quad (14)$$

Where:

$$I_{\min} = \frac{2 \cdot P_o}{V_p} \quad (15)$$

3. Determination of resonant circuit:

The value of L_{r1} and C_{r1} are obtained through the following relations:

$$\frac{L_{r1}}{C_{r1}} = \left(\frac{\alpha \cdot V_o}{I_{\min}} \right)^2 \quad (16)$$

$$L_{r1} \cdot C_{r1} = \left(\frac{1}{2 \cdot \pi \cdot f_o} \right)^2 \quad (17)$$

4. Determination of the maximum and minimum switching frequency.

The maximum switching frequency will occur at the zero-crossing of the input current. Thus, at this point, the switching frequency will be equal to the resonant frequency.

$$f_{s\max} = f_o \quad (18)$$

The minimum switching frequency will occur at the peak of the input voltage.

$$f_s(\theta) = \frac{2\pi \cdot f_o \cdot \alpha \cdot (a - \sin(\theta))}{a \cdot \left[\alpha^2 \cdot (\cos(\theta)^2 - 1) + \alpha \cdot \sin(\theta) \cdot (\sin^{-1}(\alpha \cdot \sin(\theta)) - 2\pi) + \sqrt{1 - \alpha^2} \cdot (1 - \cos(\theta)^2) - 1 \right]} \quad (19)$$

Thus:

$$f_{s\min} = \frac{2\pi \cdot f_o \cdot \alpha \cdot (a - 1)}{a \cdot \left[-\alpha^2 + \alpha \cdot (\sin^{-1}(\alpha - 2\pi)) + \sqrt{1 - \alpha^2} - 1 \right]} \quad (20)$$

5. Input Inductance

The input inductance is obtained through the following expression:

$$L_{in} = \frac{V_p}{\Delta I_{Lin_{\max}}} \cdot \frac{1}{\omega_o} \cdot \left\{ \alpha + 2\pi - \sin^{-1} \alpha + \frac{1 - \sqrt{1 - \alpha^2}}{\alpha} \right\} \quad (21)$$

6. Determination of the maximum and minimum conduction time of the switches

The maximum and minimum on-time of the switches are defined by the following expressions:

$$t_{on\min} = \frac{1}{\omega_o} \left\{ \alpha + \pi + \sin^{-1} \alpha \right\} \quad (22)$$

$$t_{on\max} = \frac{1}{\omega_o} \left\{ \alpha + 2 \cdot \pi - \sin^{-1} \alpha \right\} \quad (23)$$

B. Design Example

1. Input Data

$$\begin{aligned} V_o &= 200V & V_{in} &= 127V & V_p &= 179.6 V \\ P_o &= 250W & f_o &= 140 \text{ kHz} \\ \Delta I_{\max} &= 0.8 A \end{aligned}$$

2. Determination of the parameter α_{\max}

$$\alpha = 0.48$$

$$I_{\min} = \frac{2 \cdot P_o}{V_p} = 2.78A$$

3. Determination of resonant circuit:

$$\frac{L_{r1}}{C_{r1}} = \left(\frac{\alpha \cdot V_o}{I_{\min}} \right)^2 = \left(\frac{0.48 \times 200}{2.78} \right)^2 = 1192.48$$

$$L_{r1} \cdot C_{r1} = \left(\frac{1}{2 \cdot \pi \cdot f_o} \right)^2 = \frac{1}{(2 \cdot \pi \cdot 140 \cdot 10^3)^2} = 1.292362 \cdot 10^{-12}$$

Thus:

$$L_{r1} = L_{r2} = 40 \mu H \quad C_{r1} = C_{r2} = 33 \text{ nF}$$

With the values of L_{r1} and C_{r1} α , Z_n and f_o are recalculated:

$$Z_n = \sqrt{\frac{L_{r1}}{C_{r1}}} = \sqrt{\frac{40 \cdot 10^{-6}}{33 \cdot 10^{-9}}} = 34.815 \Omega$$

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{r1} \cdot C_{r1}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{40 \cdot 10^{-6} \cdot 33 \cdot 10^{-9}}} = 138.5 \text{ kHz}$$

$$\alpha = \frac{Z_n \cdot I_{\min}}{V_o} = \frac{34.815 \times 2.78}{200} = 0.484$$

4. Determination of the maximum and minimum switching frequency.

$$f_{s\max} = f_o = 138.5 \text{ kHz}$$

$$f_{s\min} = 16.3 \text{ kHz}$$

5. Input Inductance

$$L_{in} = \frac{V_p}{\Delta I_{Lin_{\max}}} \cdot \frac{1}{\omega_o} \cdot \left\{ \alpha + 2\pi - \sin^{-1} \alpha + \frac{1 - \sqrt{1 - \alpha^2}}{\alpha} \right\}$$

$$L_{in} = 1.6 \text{ mH}$$

6. Maximum and minimum conduction time of the switches

$$t_{on\min} = \frac{1}{\omega_o} \left\{ \alpha + \pi + \sin^{-1} \alpha \right\} = 4.74 \mu s$$

$$t_{on\max} = \frac{1}{\omega_o} \left\{ \alpha + 2 \cdot \pi - \sin^{-1} \alpha \right\} = 7.2 \mu s$$

Thus, the conduction time chosen for the switches will be 5.5 μs .

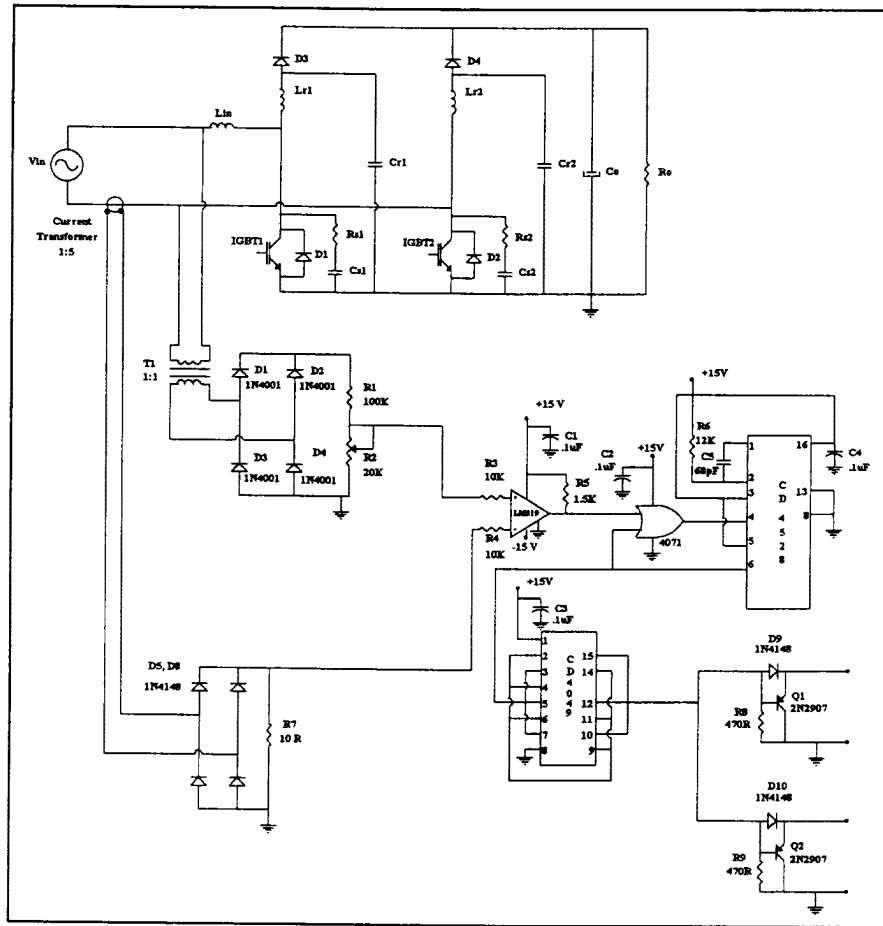


Fig. 7 - Complete diagram of the ZCS-HPF rectifier.

V. EXPERIMENTAL RESULTS

In order to experimentally verify the principle of operation and the theoretical analysis, a 250W, Quasi-Resonant ZCS high power factor converter has been implemented in laboratory. The prototype was tested with an input voltage of 127 V_{rms} and an output voltage of 200 V_{DC}.

The complete diagram of the prototype is shown in Fig.7, whose power components specification is as follows:

- IGBT₁, IGBT₂ - APT 40GF100
- D₁-D₄ - APT 15D100K
- L_{in} - 1.6 mH - 85 turns (2x15 AWG) on EE-65/26 core
- L_{r1}, L_{r2} - 40 μH - 19 turns (19x27AWG) on EE-30/14 core
- C_{r1}, C_{r2} - 33nF/630 V (polypropylene)
- C_o - 680μF
- R_{s1}, R_{s2} - 1KΩ/0.5 W
- C_{s1}, C_{s2} - 1nF/630 V (polypropylene)

A small R-C circuit composed by (R_{sn}, C_{sn}) was placed in parallel with each IGBT in order to minimize the voltage oscillations caused by the reverse recovery of D₁ and D₂.

The signal generated by the current transformer is compared with the current reference, which is generated by a

signal transformer. The result of this comparison, along with a monostable circuit will generate the drive signals to both IGBT's.

The input voltage and input current for the prototype operating at 250 W are presented in Fig. 8. The THD of the input voltage is about 4.4%. Therefore, this distortion will be present in the input current also. The power factor obtained for 250W and neglecting the high order harmonics was 0.998 with a THD of 4.6% in the input current.

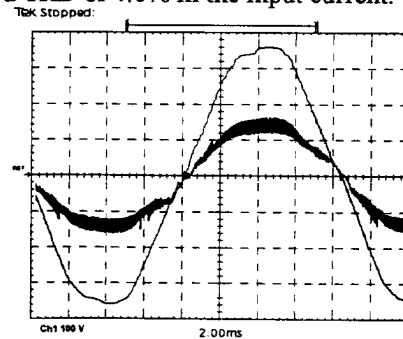


Fig. 8 - Input Voltage Vin (100V/div) and input current Iin(2A/div).
Time scale : 2.0 ms/div

The commutation of IGBT₁ is shown in Fig. 9. It can be observed that the zero-current-switching is accomplished.

The maximum voltage across the IGBT is equal to the output voltage (200 V). However, due to the reverse recovery of the anti-parallel diode, there is an overvoltage across the IGBT. The maximum switching frequency measured was 94.3 kHz and the minimum switching frequency measured was around 16.1 kHz

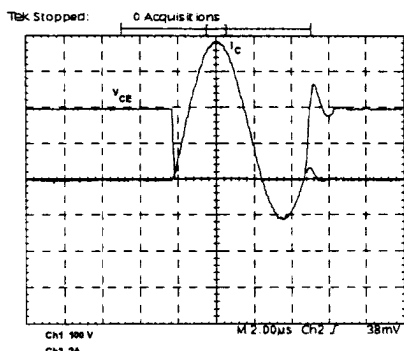


Fig. 9 - Commutation detail in IGBT₁. Collector-to-Emitter voltage VCE (100 V/div). Collector current IC (2A/div). Time scale : 2μs/div.

The voltage across the IGBT₁ and the current through the IGBT₁ and the anti-parallel diode over a AC mains cycle are shown in Fig. 10. It can be observed that during half line-cycle the current flows through the anti-parallel diode and during the other half line-cycle the IGBT₁ performs the boost function.

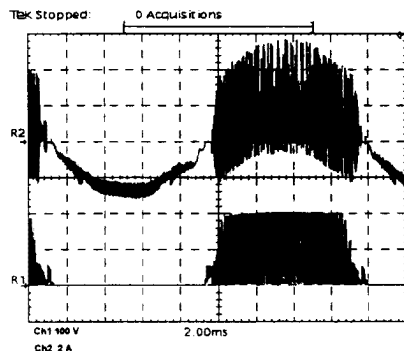


Fig. 10 - Upper trace: IGBT₁ plus diode D₁ current (2A/div). Lower trace : Collector-to-Emitter voltage VCE (100 V/div). Time scale : 2ms/div.

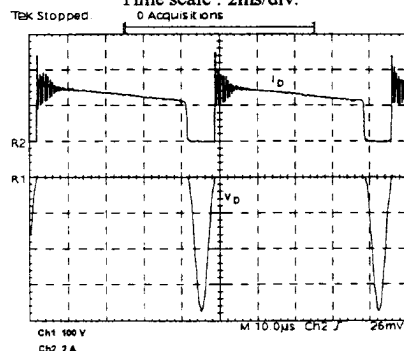


Fig. 11 - Upper trace : Current through D₃ (2A/div) Lower trace : Voltage across D₃ (100 V/div) Time scale : 10μs/div.

The voltage and current across the diode D₃ is presented in Fig. 11. It can be noticed that this diode must have a breakdown voltage larger than twice the output voltage.

VI. CONCLUSION

In this paper a new technique to improve the efficiency of power factor correction rectifiers is presented. The high efficiency is obtained due to the following factors:

- the Zero-Current-Switching;
- there are only two semiconductor voltage drops in the current flow path at any time;

Besides these two characteristics, one important advantage is that there is no auxiliary switch to perform the soft-commutation. Therefore there will not be any additional losses.

Another features of this converter include:

- Current-Sense Frequency control to achieve a high power factor,
- the voltage stresses in the switches are fixed for all load conditions. The voltage in the main switches is clamped on the output voltage. However the diodes must be dimensioned to the double of the output voltage.

This new converter is suitable for high power applications employing IGBT's due to two important facts:

- IGBT's devices are more appropriated for the ZCS commutation;
- the quasi-resonant characteristic of the current in the switches presents a high rms value. However the conduction losses in IGBT's are proportional to the average current flowing in the device, which are lower.

REFERENCES

- [1] R. Streit and D. Tollik, "High Efficiency Telecom Rectifier Using a Novel Soft-Switched Boost-Based Input Current Shaper", *EEE INTELEC Records*, 1991, pp. 720-726.
- [2] G. Hua, C.S. Leu, and F.C. Lee, "Novel Zero-Voltage-Transition PWM Converters", *IEEE PESC Records*, 1992, pp. 55-61.
- [3] I. Barbi and S. A. O. da Silva, "Sinusoidal Line Current Rectification at Unity Power Factor with Boost Quasi-Resonant Converters", *IEEE APEC Records*, 1990, pp. 553-562
- [4] P.N. Enjeti and R. Martinez, "A High Performance Single-Phase AC to DC Rectifier with Input Power Factor Correction", *IEEE APEC Records*, 1993, pp. 190-196.
- [5] A.F. Souza and I. Barbi, "A New ZVS-PWM Unity Power Factor Rectifier with Reduced Conduction Losses", *IEEE PESC Records*, 1994, pp. 342-348.