

Application of a Generalized Current Multilevel Cell to a Current Source Inverter

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Abstract - In this work a new cell which lends itself as a generic current multilevel one is applied to a five level current source inverter (CSI) with output current harmonics minimization and without the use of high frequency modulation. In this cell, inductors acting as current sources ensure equal current division among switches. DC current balance in the inductors is achieved also without closed-loop control. Two switching strategies are used to demonstrate the performance of the cell. The first switching strategy is called symmetric strategy. The second one, called asymmetric strategy is suggested by the authors. A comparison between the two strategies is also made. Simulation and experimental results are included to show the performance of the new cell in a current source inverter for high power applications.

1. INTRODUCTION

The conventional association of semiconductor switches in series or in parallel became a common practice in the power electronics field constituting, even nowadays, an object of several scientific papers [1], [2]. These procedures give feasibility to high voltage or high current applications for which no single actual switch is able to operate. However, depending on the application and on the nature of the adopted semiconductor device a number of requirements must be observed in order to ensure a reasonable reliability in using those technologies. An alternative to the simple association of switches is the association of converters. This technique can provide not only high power applications but also a reduction of the harmonics content. Under this concept it is possible to associate current source inverters in series [3] or in parallel [4]. Similarly, one can associate voltage source inverters in series [5] or in parallel [6]. Another recent approach in the high power converters study changes the association of converters concept into a more general principle, by making the association of PWM cells [7]. This concept has generated the multilevel converters designation and has been extensively used to reduce the harmonic distortion of a converter, as well as to provide high voltage distribution among the employed cells [8]. Most of those publications have been focused the series association of cells in such a great deal that resulted in a proposed generic multi-

level voltage cell [9], [10]. An alternative to increase the power capability of these converters, by paralleling the PWM cells, has also been proposed [11]. It seems that until now the multilevel concept has only been used to voltage source converters, meaning a suitable way to divide the total input voltage among a number of employed PWM cells and also allowing voltage harmonics reduction.

In this work a recent introduced generic current multilevel cell [12] is reshaped and adapted to be used in a five level current source inverter. Appropriate gating strategies provide for this new structure a balanced distribution of the input current among the employed switches and an output current with elimination of some harmonic components, without the use of high frequency modulation or closed-loop control.

The original current multilevel cell is shown in Fig.1, where between the point A and P there is a voltage source (or a capacitive branch) and at point C a current source (or an inductive loop). This cell employs n PWM switches (indicated by dashed lines) that are connected by $n-1$ inductors which provide the current multilevel feature. This generic cell can be used in any PWM voltage-source converters (dc-dc converters and VSI inverters). Depending on the nature of the output current and on the type of the final converter the PWM cells can be constituted of a variety of controlled and non-controlled switches arrangements. In a buck converter, for example, the upper switch is a controlled one and the lower switch is a simple diode.

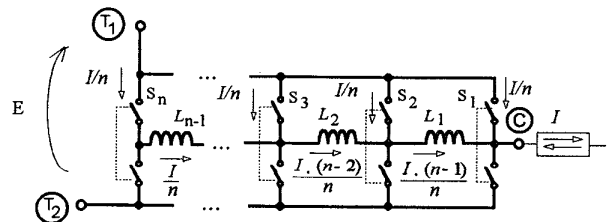


Fig.1 The original generic cell

The generic current multilevel cell is reshaped in Fig.2 becoming a generic current inverter cell. Also the PWM switches have been adapted to a current source input, acting

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as a voltage bi-directional/current unidirectional switch. Now, the generic cell is ready to be used in any current-source PWM converter, such as a current source inverter.

2. THE FIVE LEVEL CURRENT SOURCE INVERTER

Using the generic structure of Fig.2 one can conceive a topology that provides up to five levels in the load current, such as the one shown in Fig.3. The PWM switches are made up of four couples of parallel complementary (PWM) switches (S_5S_6 ; S_7S_8 ; S_1S_2 and S_3S_4).

To guarantee the source current is equally divided between any two switches of the cell (S_5 and S_7 , for example), it is necessary, but not sufficient, that they have the same duty cycle and the same on resistance. If they switch on and off at the same time, the switches could be associated as seen in Fig.4(a), where r_s represents the switch resistance and L a lossless inductor.

However, to provide stepped waveform and consequently harmonic reduction in the load current it is necessary one of the switches be on while the other one is off. This situation causes an alteration in the parallel path of Fig.4(a) since the load branch Z_L (that is., R_L/C_L) is going to be present in one of the paths. Suppose S_5 is on and S_7 is off. Because of the complementary operation of the switches, S_8 is on and S_6 is off. One possible mesh for the current I to flow is shown in Fig.4(b).

It is easy to conclude that, in steady state, the current is going to be larger through S_5 than through S_8 if the imbalance situation described above is not compensated. To avoid this problem two switching strategies are proposed as follows.

3. SYMMETRIC SWITCHING STRATEGY

In this strategy the switches operate with a duty cycle of 50%, as shown in Fig.5. A similar procedure has been proposed to the structure in [4], as discussed in [13]. In this figure the parameter α is the angle associated to the time conduction delay between two switches of any inverter branch (S_1 and S_3 , S_6 and S_8 , etc.), θ_1 is the common conduction angle of any two switches of the external arms (S_3 and S_5 or S_4 and S_6) and θ_2 is the common conduction angle of any two switches of the internal arms (S_1 and S_7 or S_4 and S_6). Note that the multilevel operation of the structure only happens for α , θ_1 and θ_2 not equal to zero. As can be seen in this figure the gate signals require two periods of the output current to complete a cycle. This constitutes a requirement in this strategy and it is employed to compensate the imbalance mentioned in the last section, as discussed at following.

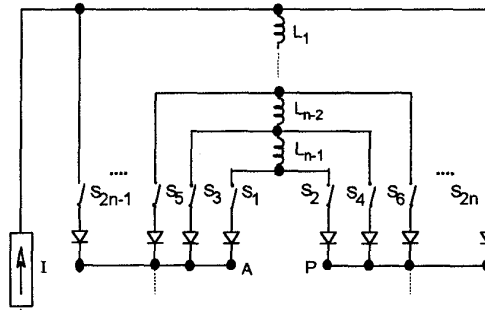


Fig.2 The generic cell reoriented

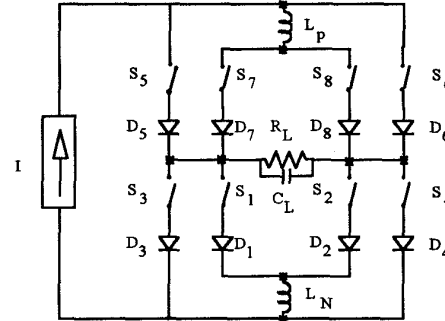


Fig.3- The Five Level Current Source Inverter

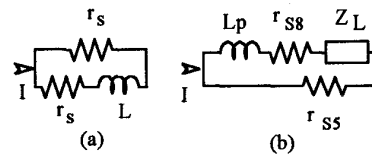


Fig.4- Parallel paths
(a) Generic representation (b) Inclusion of the load branch

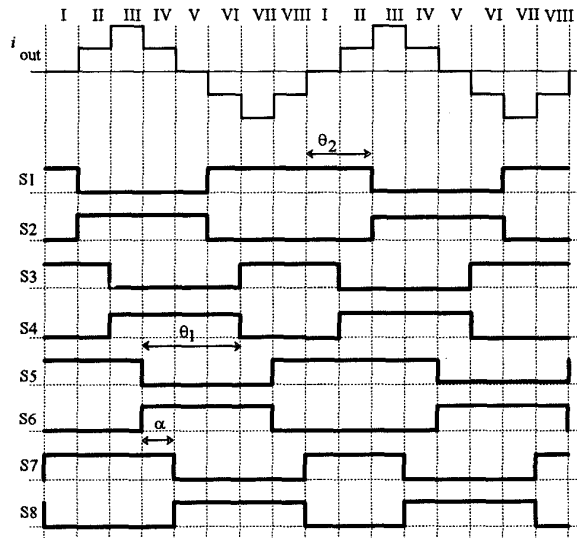


Fig.5 Symmetric switching strategy

The analysis of the first eight intervals of Fig.5 shows that inductor current balance cannot be reached for one period of the output current, as analyzed in Fig.6 for some selected intervals.

From the circuits of Fig.6 one can conclude that the load impedance, when present in one of the branches of the cell, is always in series with the sharing inductance. That makes, in steady state, the inductance current be smaller than the one of that in the other branch. To overcome this imbalance a switching sequence can be chosen such that the load resistance, during the intermediate levels, is in the branch with no sharing inductance. Consider the Interval II, the two paths are made of S_5S_7 and S_3S_2 . The same output current could be obtained with the switches S_5S_7 and S_4S_1 , and so on for the other intervals. The two switching sequences are used as shown in Fig.5. Assuming negligible ripple one can consider $I_{LP}=I_{LN}$. The switching sequence is going to depend on the values of θ_1 , θ_2 and α . For θ_1 , θ_2 and α of Fig.5 the first period of the output current was provided by the following sequence: $S_5S_7S_1S_3$, $S_5S_7S_2S_3$, $S_5S_7S_2S_4$, $S_6S_3S_2S_4$, $S_6S_8S_2S_4$, $S_6S_8S_1S_4$, $S_6S_8S_1S_3$ and $S_5S_8S_1S_3$. The same output current waveform could be obtained with the following sequence: $S_5S_7S_1S_3$, $S_5S_7S_1S_4$, $S_5S_7S_2S_4$, $S_5S_8S_2S_4$, $S_6S_8S_2S_4$, $S_6S_8S_2S_3$, $S_6S_8S_1S_3$ and $S_6S_7S_1S_3$.

Any of those sequences alone cannot produce a current balance in the cell. However, when one is used after the other, consecutively, as shown in Fig.5, the result is an equilibrium in the steady state current of the cell. Of course the ripple in the inductors current must be small, and it is going to depend on the values of L , α , θ_1 and θ_2 .

A. Load Current Control

The contributions of the outer and inner inverters, associated to the angles θ_1 and θ_2 , can be thought as two individual currents, i_1 and i_2 , that should be added to result in the output current i_{out} . The equations below describe the rms values of the individual contributions.

$$I_1 = \sqrt{\left(1 - \frac{\theta_1}{\pi}\right)} \cdot \frac{I}{2} \quad (1)$$

$$I_2 = \sqrt{\left(1 - \frac{\theta_2}{\pi}\right)} \cdot \frac{I}{2} \quad (2)$$

As the cell supplies I_1+I_2 to the load, and I_1 and I_2 are out of phase by α , the rms value of the output current is given by

$$I_{out} = \sqrt{I_1^2 + I_2^2 + 2I_1I_2 \cos \alpha} \quad (3)$$

Equation (3) shows clearly the dependence of the output current magnitude due to the angle parameters. If $\theta_1=\theta_2=\theta$ one can get

$$I_{out} = \sqrt{\frac{2}{\pi}} \cdot \frac{I}{2} \cdot \sqrt{(1 - \cos \alpha) \cdot (\pi - \theta)} \quad (4)$$

The harmonic spectrum of i_{out} changes considerably for different values of α , θ_1 and θ_2 . From [8], it can be shown that choosing proper α , θ_1 and θ_2 two harmonic components may be canceled.

For $\theta_1=\theta_2=60^\circ$ and $\alpha=30^\circ$, the output current is a five level current wave in which the 3rd is eliminated and the 5th harmonic component is very small, as seen in the following simulation results.

B. Symmetric Switching Strategy-Simulation Results

The performance of the five level structure, driven by the symmetric strategy, and for $\theta_1=\theta_2=60^\circ$ and $\alpha=30^\circ$ is shown in the next figures with the following parameters:

$$L_p = L_n = 50mH, r_{on} = 0.1\Omega, r_{off} = 10^6\Omega, \\ R_L = 6.3\Omega, C_L = 100\mu F \text{ and } I = 18A.$$

Fig.7 to 9 show the simulation results for the above set of parameters. From Fig.7 one can see a good current distribution among switches.

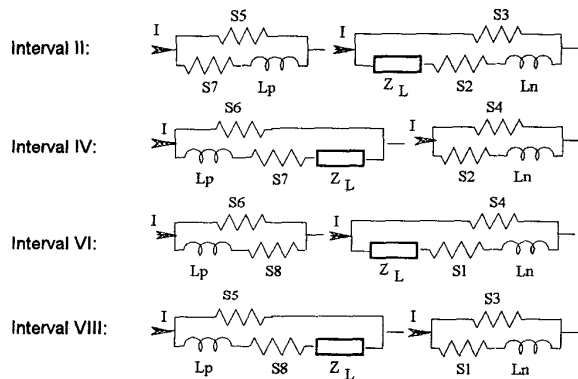


Fig.6 Intervals in which the load impedance is part of the cell

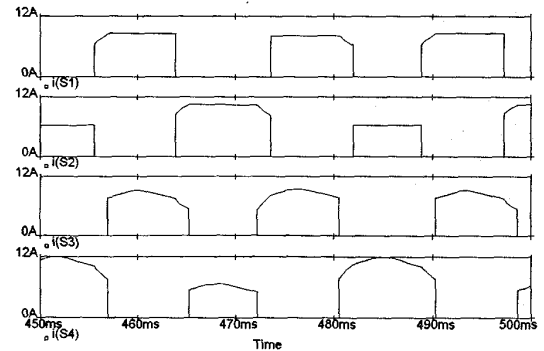


Fig.7-Current in the switches of some cells

In Fig.8 it is shown the waveforms for the balance inductor currents as also the voltage and current at the output of the structure. Fig.9 shows the output current harmonic spectrum, where can be noticed a good low order harmonics minimization. The harmonic distortion factor is 12.1%. A smaller index can be computed for the filtered output voltage: 7.4%.

4. ASYMMETRIC SWITCHING STRATEGY

Although the symmetric strategy has the advantage of working with 50% duty cycle for any output power or harmonic spectrum, it contributes for the increase of the current ripple in the sharing reactors, and, as a consequence, a higher current imbalance in the switches of the cell. This happens because it is needed two periods of the output current, as shown in Fig.5, to make the average sharing inductor voltage equal to zero. That current ripple is given by:

$$\Delta I = \frac{V_{out}}{L} \cdot \Delta t \quad (5)$$

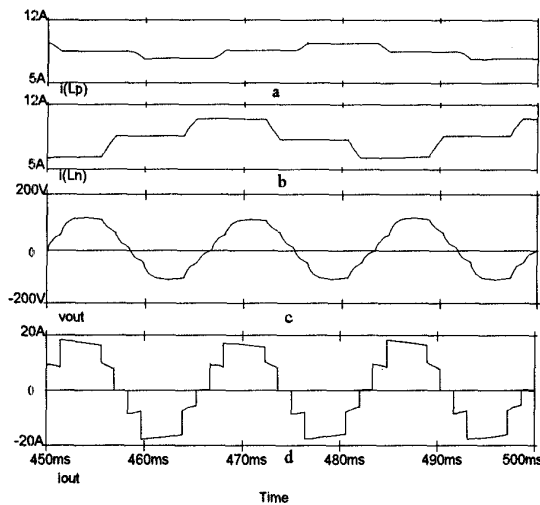


Fig.8 (a) Current in inductance Lp (b) Current in inductance Ln (c) Load Voltage (d) Output Current

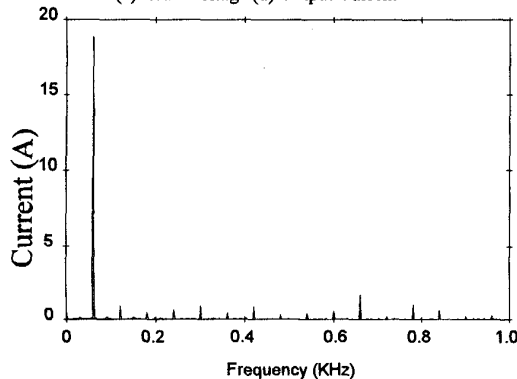


Fig.9 Output Current Harmonic Spectrum

Where Δt is the interval when a balance inductor, $L=L_P=L_N$ is subjected to the output voltage, V_{OUT} (here assumed constant during this interval). The symmetric switching strategy shown in Fig.10 for $\theta_1=\theta_2=60^\circ$ and $\alpha=30^\circ$, reduces the current ripple in the sharing reactors by half because it makes the average voltage of the inductors equal to zero for one period of the output current. The only inconvenience of this strategy is the asymmetric operation of the switches. However, for low order harmonic elimination the difference in the switches duty cycles is no more than 15%, when compared with the 50% duty cycle of the symmetric one. To see how this strategy works it is necessary to analyze two intervals: II and VI.

In interval II the switches in operation are S_4S_2 and S_6S_7 . The load impedance is in series with inductor L_p and S_7 . This would lead, in steady state, to an inductor current smaller than $I/2$. However, in interval VI the switches in operation are: S_3S_1 and S_6S_7 , the load impedance is, now, in series with switch S_6 only. This increase the inductor steady state current to a value higher than $I/2$. As long as the time duration of interval II is the same of interval VI, apart from the ripple in the inductor current, its average current is $I/2$. The same analysis can be made for the intervals IV and VIII, and the conclusion is that the average branches impedances are the same for one period of the output voltage.

A. The Load Current Control

The magnitude is controlled by changing the angle φ , as defined in Fig.10. The output current is maximum for $\varphi=0$. Naturally the harmonic spectrum of i_{out} changes considerably for different values of φ .

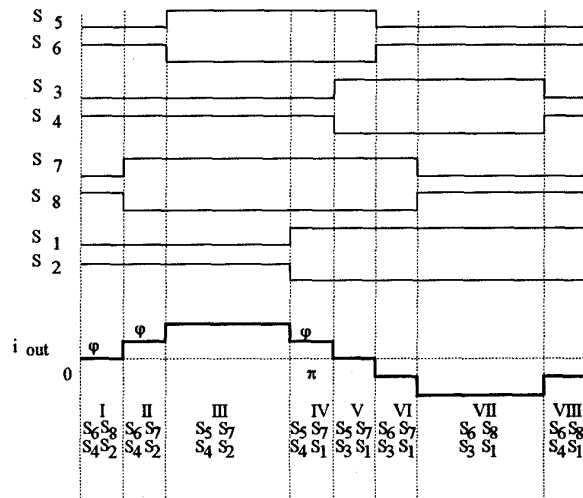


Fig.10 Asymmetric switching strategy for output current harmonic reduction

The rms value of the output current is given by

$$I_{\text{out}} = \left[\frac{1}{\pi} \left(\int_{\varphi}^{2\varphi} \left(\frac{I}{2}\right)^2 d\omega t + \int_{2\varphi}^{\pi-\varphi} I^2 d\omega t + \int_{\pi-\varphi}^{\pi} \left(\frac{I}{2}\right)^2 d\omega t \right) \right]^{1/2}, \quad (6)$$

$$I_{\text{out}} = I \sqrt{1 - \frac{5\varphi}{2\pi}}. \quad (7)$$

B. Simulation Results

The behavior of the structure driven by the asymmetric switching strategy is seen in Fig.11 and Fig.12. It can be noted the smaller ripple current in the sharing inductors, when compared to the symmetric strategy in Fig.8. That is important for the current balance in the switches of the cell. The ripple for the asymmetric strategy is half of that for the symmetric one as show the simulation results. It has been considered the same parameters for symmetric and The simulated harmonic spectrum of the output current is very close of that in Fig.9. The output voltage harmonic distortion is 6.1%.

5. LABORATORY PROTOTYPE

To validate the use of the cell and to check out the simulation results a laboratory prototype has been designed and constructed as represented in Fig.13. It has to be point out that, due to the low frequency operation of the structure (60Hz) and the non simultaneous operation of the switches, it was necessary a sharing inductance with a value of 45mH. The inductor was made with silicon steel and its wiring resistance measured 0.3Ω. In order to ensure a good current distribution the balance inductor resistance must have a value much smaller than the ON resistance of the switches.

In the experimental setup IGBT's were used as active switches. It is interesting to note, however, that it would be a smart choice to use GTO's instead of IGBT's, since no diodes would be necessary. Unfortunately, at the laboratory implementation time this choice could not be made.

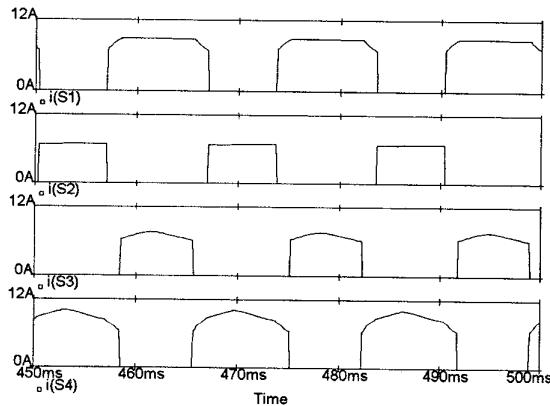


Fig.11. Current in the switches of two cells

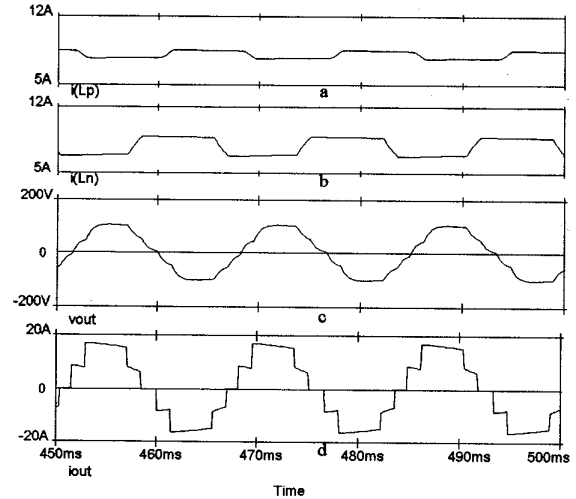


Fig.12- Simulation results for the asymmetric strategy. (a) Current in Lp (b) Current in Ln (c) Load Voltage (d) Output Current

The employed IGBT's have an ON resistance of 0.12Ω, therefore smaller than that of the balance inductor. This is the reason for the inclusion of the small resistors, r_1 and r_2 , as shown in Fig.13. Of course these resistors will cause a decrease on the converter efficiency. For the adopted set of parameters this reduction was about 4%, what could be smaller if a better technique had been used to implement the balance inductors.

Both switching strategies were stored in an EPROM where a bit enables one or other strategy at the data bus. Each each bit of the data bus is a 60Hz signal for the eight controlable switches. Finally, the gate signals are isolated and stepped up to 13V by a pulse transformer-isolated circuit.

The measured output power for the structure in Fig. 13 was 1.2kW. The input current source was obtained from a dc voltage source, V_i , in series with a 105mH inductor. Fig.14 shows the current in the switches of the structure for the asymmetric strategy.

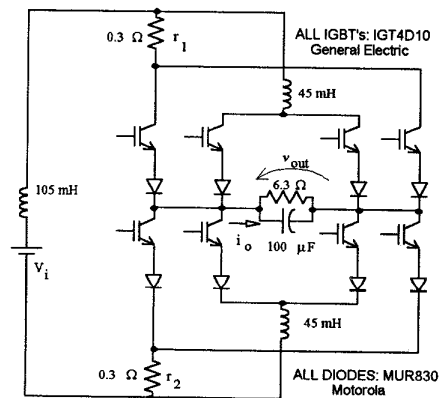


Fig.13- Power circuit of the experimental setup

Fig.15 shows the five level inverter output voltage and current. The load is made of a parallel RC combination, being $R=6.3\Omega$ and $C=100\mu F$. The harmonic analysis yields a 5.5% and 15.5% total harmonic distortion for the output voltage and current, respectively. The current ripple in the sharing reactors is shown in Fig.16 for both strategies.

6. CONCLUSION

The application of a new current multilevel cell to a current source inverter structure has been presented. The concept of current multilevel converters has been introduced here. The main advantages in the use of the new cell are the possibility of generalization to n-level in the output current and the need of less sharing reactors than other structures known. The concept can be extended to a number of other converters, such as PWM dc-dc converters. With proper switching strategy it is possible to reduce the size of the sharing reactors and eliminate some harmonics of the output current without the use of high frequency modulation. All these advantages suggest the use of the structure in high power applications.

7. ACKNOWLEDGMENT

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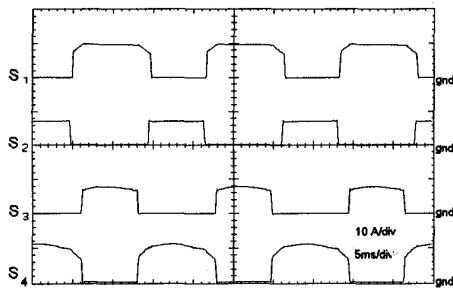


Fig.14- Current in the switches - Asymmetric strategy

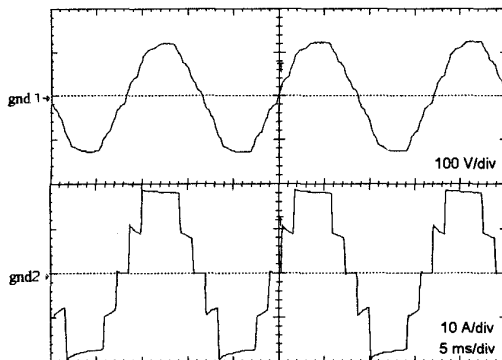


Fig.15- Output voltage(top trace) and current

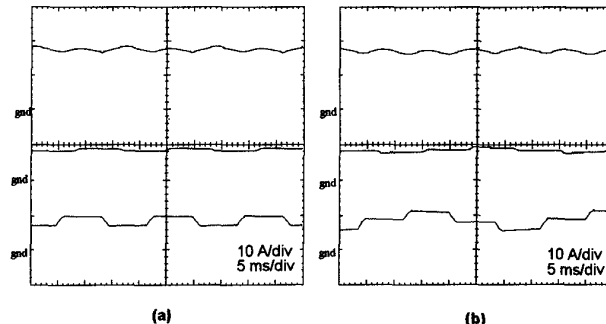


Fig. 16- Input current(top trace), I_{LP} (middle trace) and I_{LN} (bottom trace). a) Asymmetric and b) symmetric strategy

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