

A NEW HIGH POWER FACTOR THREE- PHASE DIODE RECTIFIER.

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Abstract - This paper proposes a new high power factor three-phase diode rectifier. The new circuit is composed of a three-phase Line Inter-phase Transformer (LIT), two three-phase diode rectifiers, followed by a PWM boost cell.

The active switch of the boost converter is gated at a constant frequency such that the AC input current is discontinuous. This procedure provides an input current shaping without the 3rd, 5th and 7th harmonics. The current that flows through the LIT and the input transformer has the switching frequency, such that ferrite cores with small size are utilized.

Besides this, the output voltage is regulated by PWM, to compensate line voltage variations and load change. The output voltage has a low practical level.

Theoretical analysis, design procedure, design example and experimental results are presented.

1. INTRODUCTION:

One of the most important research topics in power electronics at the present time is the power factor correction of three-phase diode rectifier with capacitive filter. This kind of rectifier is the most utilized in industrial and commercial applications for economic reasons. The technique proposed in reference [1] and shown in Fig.1 is very simple because it uses only one active switch, with no active control of the current. Due to its simplicity, it is one of the most popular techniques discussed in the literature. In this circuit, the input current shaping is achieved thanks to the discontinuous inductor current mode.

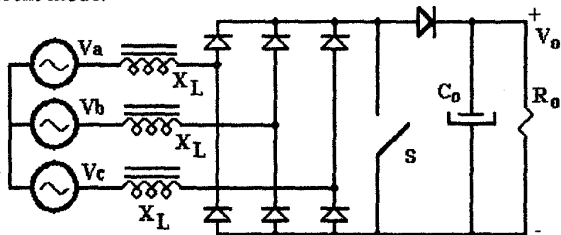


Fig.1 High power factor three-phase diode rectifier proposed in [1]

Two main drawbacks of the mentioned converter have been identified; namely excessive output voltage and the presence of 5th harmonic in the line current.

A less known but not less important power correction technique, suitable for high power application was proposed in reference [2] and represented in Fig. 2.

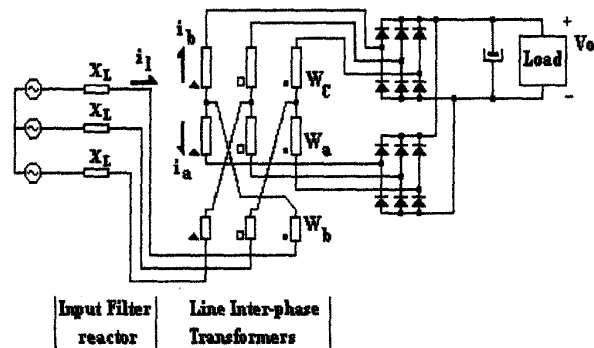


Fig.2. High power factor three-phase diode rectifier using the LIT proposed in [1].

This technique is simple, offers high reliability, and the most important, has been used successfully in many industrial applications.

Four problems could be mentioned, about this converter: the first one is the fact that the output voltage is not controlled; the second is that it is low for most applications; the third one is that the Line Inter-phase Transformer are relatively large because they operate at the line frequency, and the fourth one, the input filter reactor cause a displacement factor.

In this paper we propose a technique that benefits from the best features of the two mentioned circuits. Details are provided in the following sections.

2. THE PROPOSED CIRCUIT

The proposed circuit is shown in Fig.3 It is formed by three boost inductor (L), a three phase Line Inter-phase Transformer (LIT) [1], two three phase diode rectifier (Ra,Rb) ,

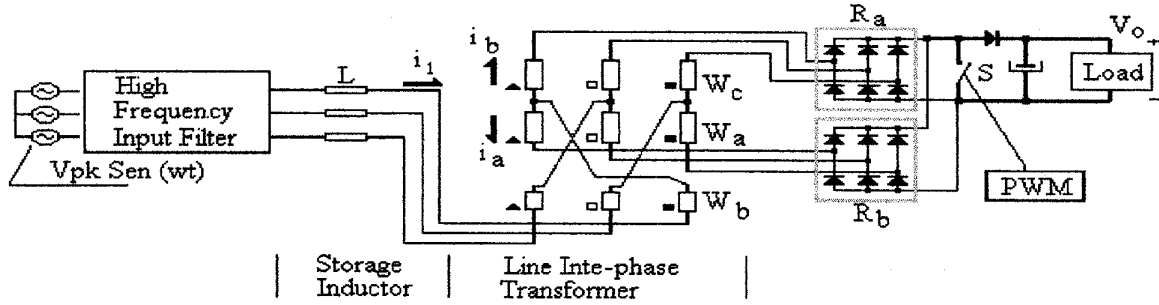


Fig. 3 Proposed circuit

followed by a PWM DC-DC boost cell. A three-phase high frequency input filter is placed between the main and the boost inductor. The LIT role is to provide a displacement of 30° between the input currents of Ra and Rb. Such displacement reduces or eliminate some low frequencies input current harmonics.

The boost converter operates at constant frequency, such that the current through L is in discontinuous current mode. As a consequence, all the magnetic components operate at the switching frequency.

The LIT winding turns-ratio to ensure 30° of displacement is given by:

$$\frac{Wb}{Wa} = \frac{\sqrt{3}-1}{2} = 0.366 \quad (1)$$

$$Wc = Wb + Wa \quad (2)$$

3. PRINCIPLE OF OPERATION

In order to simplify the analysis, it is assumed the following:

-The switching frequency is much higher than the line frequency.

- The semiconductors are ideal.
- The transformers have negligible magnetizing current .
- The output circuit has a large capacitor.
- The phase sequence is positive (abc)

The circuit presents twelve topological groups of combinations in half line wave. The operation of the converter is cyclically repeated every 30°. Therefore its operation is completely characterized when the interval from zero up to 30° is described.

3.1 STAGES OF OPERATION FROM 0° ≤ θ ≤ 15°

a) First stage: (Energy storage, Fig 4

During this stage the switch S is kept closed. The LIT secondary windings are short-circuited via the rectifiers Ra and Rb, the boost inductor current raises linearly. The equivalent circuit is shown in Fig. 4 b.

b) Second stage: (First power transfer stage, Fig. 5)

During this second stage, the switch S is off. Due the presence of the LIT, the current i_{La} continues rising linearly while the currents i_{Lb} and i_{Lc} start decreasing linearly. This stage ends at the instant that current through the winding Wa reaches zero.

c) Third stage: (Second power transfer stage, Fig. 6)

During this stage the boost inductor current decreases linearly and reaches zero simultaneously.

d) Fourth stage: (zero inductor currents, Fig. 7)

During this stage all inductor currents are equal to zero.

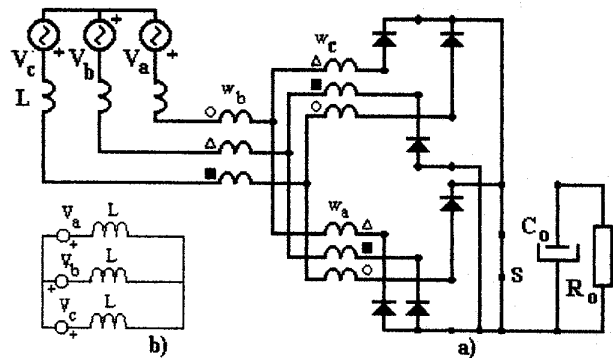


Fig. 4 Equivalent circuit for the first stage of operation, for 0° ≤ θ ≤ 15°. Switch S is closed.

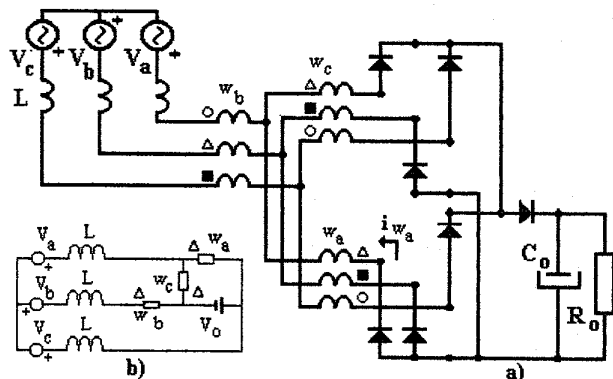


Fig. 5 Equivalent circuit for the second stage of operation, for 0° ≤ θ ≤ 15°. Switch S is opened.

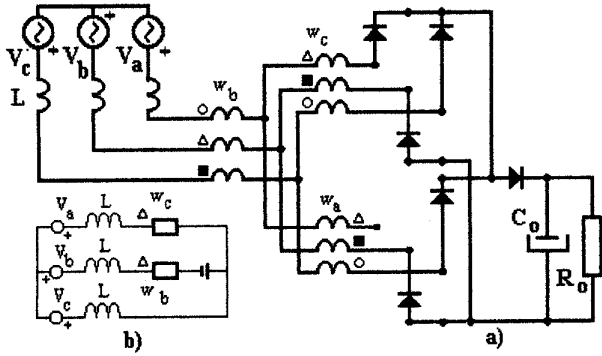


Fig. 6 Equivalent circuit for the third stage of operation, for $0^\circ \leq \theta \leq 15^\circ$. Switch S is opened.

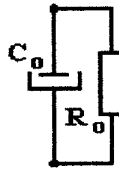


Fig. 7 Equivalent circuit for the fourth stage of operation. All inductor boost currents are kept null.

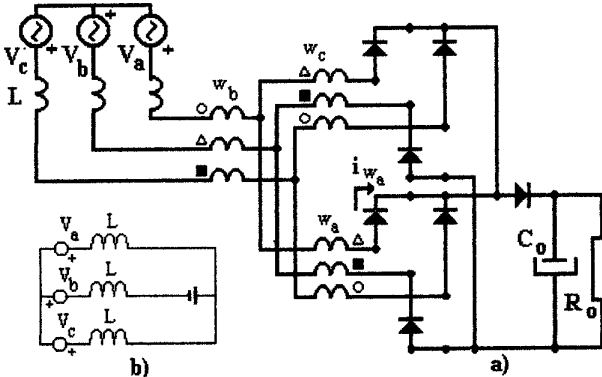


Fig. 8 Equivalent circuit for the second stage of operation, for $15^\circ \leq \theta \leq 30^\circ$. Switch S is opened.

3.2 STAGES OF OPERATION FROM 15° TO 30°

a) First stage: (Energy storage)

During this stage the switch S is kept closed, and the boost inductor current raises linearly again. The equivalent circuit is equal to Fig. 4 b.

b) Second stage: (First power transfer stage, Fig. 8)

During this second stage, the voltage across the LIT windings is equal to zero, all current decrease linearly. This stage ends at the moment that current through the winding W_a becomes zero.

c) Third stage: (Second power transfer stage, Fig 6)

During this stage all boost inductor currents decrease linearly. It finishes when the three currents become zero simultaneously.

d) Fourth stage: (zero inductor currents, Fig. 7)

During this stage all inductor currents are equal to zero. The Fig. 9 and Fig. 10 b show the inductors current for $0^\circ \leq \theta \leq 15^\circ$ and $15^\circ \leq \theta \leq 30^\circ$, respectively.

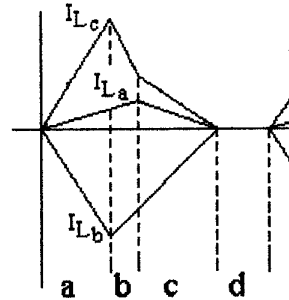


Fig 9 Inductors current for $0^\circ \leq \theta \leq 15^\circ$.

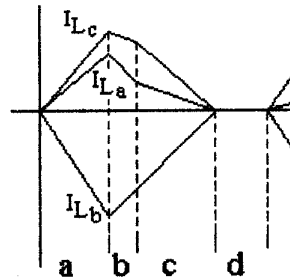


Fig 10 inductors current for $15^\circ \leq \theta \leq 30^\circ$

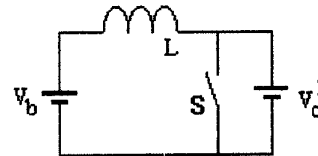


Fig.11 Equivalent monophasic circuit for critical situation.

$$V_o^1 = \frac{(2 + \sqrt{3})}{6} V_o \quad (3)$$

$$V_b = \frac{(\sqrt{6} + \sqrt{2})}{4} V_{pk} \quad (4)$$

4 RELEVANT ANALYSIS RESULT

An analysis was made doing an equivalent monophasic circuit for critical situation. (Fig 11.). By analytical and numerical approach, the most relevant curves representing the behavior of the output characteristics are shown in Fig. 12. They represent the output voltage versus the output current, taking the duty cycle as a parameter. The power factor and the THD are shown in Figures 13 and 14 respectively.

The voltage ratio is defined as follows:

$$\beta = \frac{V_o}{V_{LL}} \quad (5)$$

$$\bar{I}_o = D^2 \frac{1}{0.789\beta - 1} \quad (6)$$

V_{LL} = rms value of the line to line voltage.
 V_o = output voltage.

Those characteristics show that the power factor is higher than 0.996 for $\beta > 1.5$ and the total harmonic distortion is very low. Besides, it still presents the characteristic of the power factor correction boost AC-DC converter.

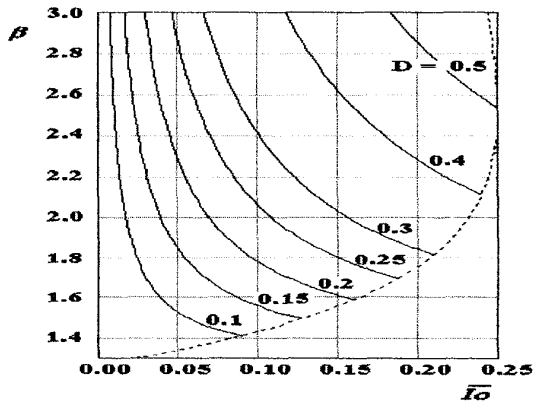


Fig. 12 Output characteristics.

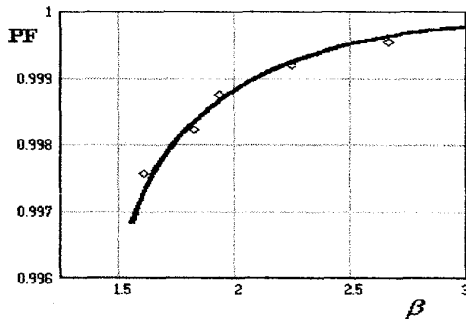


Fig. 13 Power factor obtained by numerical analysis.

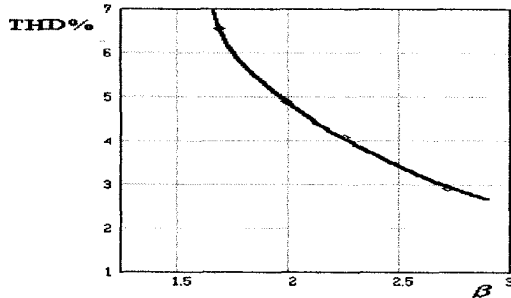


Fig. 14. THD obtained by numerical analysis.

To obtain the similar PF by [1], the output voltage must be very high, moreover, to low PF in [1] the output voltage is high, also. For the proposed circuit, the output voltage is low when compared to [1].

5 DESIGN PROCEDURE

A simple procedure is presented for the components specification of the proposed topology.

- With β from (5), in Fig. 12 the normalized output current and the maximum duty cycle (D_m), can be obtained.

- With the output power, normalized output current and efficiency, using (7), it is obtained the maximum inductor (L) that warrants DCM mode.

$$L = 0.38 \frac{V_o^2 \cdot \eta \cdot \bar{I}_o}{\beta \cdot P_o \cdot f_s} \quad (7)$$

-With the established inductor, the peak switch current is given by

$$I_{pk} = 0,816 \cdot \frac{V_{LL}}{L \cdot f_s} \cdot D_{max} \quad (8)$$

-With D_m and the output current, is obtained the current stress, from (9), (10), (11) and (12) and figures 15, 16 and 17.

Average and RMS switch current

$$I_{Sef} = \bar{I}_{Sef} \cdot I_o \quad I_{Sm} = \bar{I}_{Sm} \cdot I_o \quad (9)$$

Total RMS output current to bridge rectifiers

$$I_{Tef} = \bar{I}_{Tef} \cdot I_o \quad (10)$$

Average diode current in bridges rectifiers

$$I_{Dpm} = 0,166 \cdot (I_o + I_{Sm}) \quad (11)$$

RMS inductor boost current

$$I_{Lef} = 0.715 \cdot I_{Tef} \quad (12)$$

-The peak voltage across the switch is given by:

$$V_{RRM} = V_o \quad (13)$$

-The LIT turns are:

- Total secondary turns

$$W_T = \frac{V_o \cdot 10^4}{\beta \cdot f_s \cdot B_m \cdot A_e} \quad (14)$$

Where:

B_m = Maximum magnetic flux density

A_e = Core Area

Primary turns:

$$W_b = 0.155 \cdot W_T \quad (15)$$

Turns of first secondary:

$$W_a = 0.423 \cdot W_T \quad (16)$$

6 DESIGN EXAMPLE

Using the following specifications:

$$V_{LL} = 220 \text{ V (60 Hz)}$$

$$V_o = 400 \text{ V}$$

$$P_o = 6000 \text{ W} \quad \eta = 0.9 \quad f_s = 26000 \text{ Hz}$$

Then,

$$\beta = 1.81 \quad \bar{I}_o = 0.20 \quad D_{max} = 0.3$$

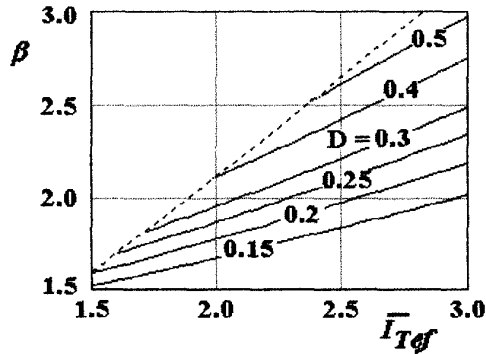


Fig. 15 Total RMS normalized current in output bridge rectifiers,

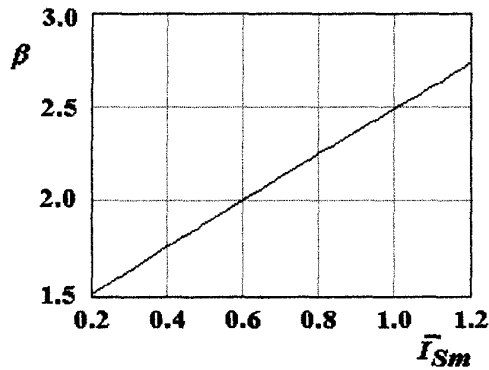


Fig. 16 Average normalized switch current.

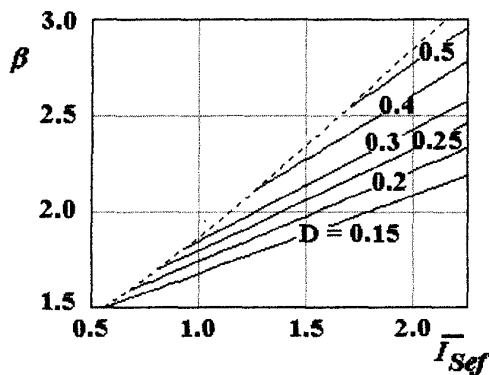


Fig. 17 RMS normalized switch current.

$$L = 37.6 \mu H \quad I_o = 15 A$$

$$\bar{I}_{Tef} = 1.7 \quad \bar{I}_{Sef} = 0.9 \quad \bar{I}_{Sm} = 0.45 \quad \bar{I}_{Def} = 1.45$$

$$I_{Tef} = 25.5 A \quad I_{Sef} = 13.5 A$$

$$I_{Sm} = 6.75 A \quad I_{Def} = 21.75 A$$

$$I_{Lef} = 18.2 A \quad I_{pk} = 54.5 A$$

Then, the semiconductors selected were:

Bridge rectifier diode = MUR1550.

Output diode = 2 x MUR1550.

Main switch = IRGPC50U (IGBT).

The windings of LIT are:

Using a core THORTON'S E65/36 IP6:

$$WT = 45 \quad W_a = 19 \quad W_b = 7$$

7 EXPERIMENTAL RESULT

A laboratory prototype has been made with the parameters and specifications obtained in Section 5:

The preliminary results are shown in Figures 18, 19, 20 and 21 to 4 kW and 400 V. Those Figures show the expected behavior, and indicate that a power factor equal to 0.998 and a THD equal to 6% have been obtained, for an output power of 4kW. It is noticed that the 3rd, 5th and 7th harmonics of the input current are eliminated. The 11th harmonic is responsible for 5% of the total harmonic distortion. The low frequency total harmonic distortion (< 11th harmonic) is due to AC mains pollution. Due to the turn off losses of DCM using IGBT's, is necessary to use soft switching to obtain the expected power.

7 CONCLUSIONS

- The preliminary experimental results illustrate an important reduction of harmonic distortion in the current, Then, the main objective has been accomplished.

- The AC mains used has a voltage distortion due to high nonlinear loads.

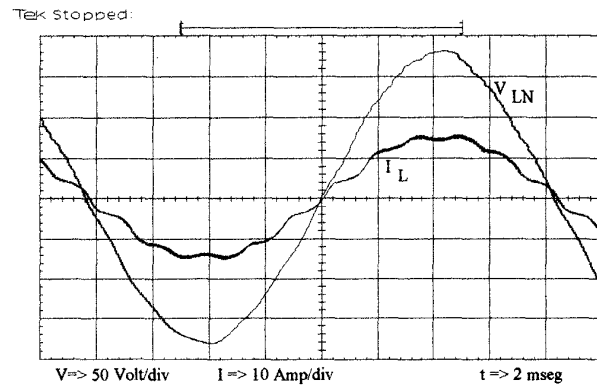


Fig. 18 Experimental line current and phase voltage

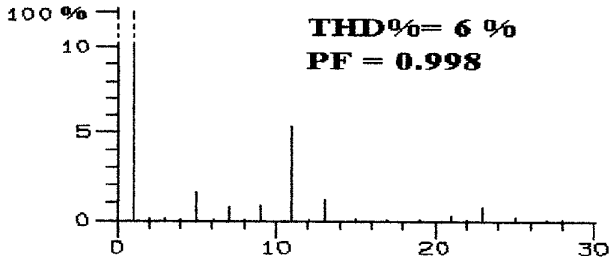


Fig. 19 Line current harmonic component.

- The total volume of the topology is very low.
- The output voltage has best behavior when compared with [1], [2].
- A very small selective filter could be used to reduce the value of 11th and 13th total harmonic distortion in order to accomplish IEC 555-2 standards.
- It's an attractive solution for high power AC-DC conversion.
- The design guidelines provide a simple procedure for the selection of components.

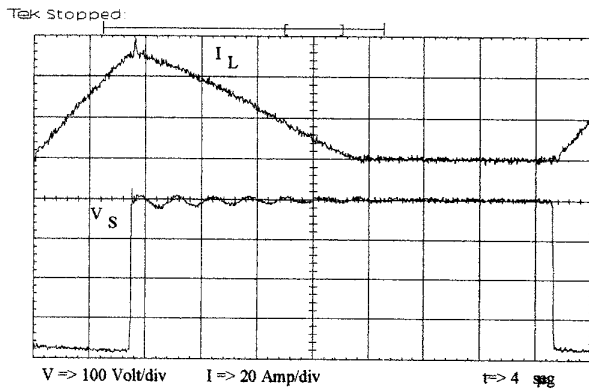


Fig 20 Experimental inductor current and switch voltage

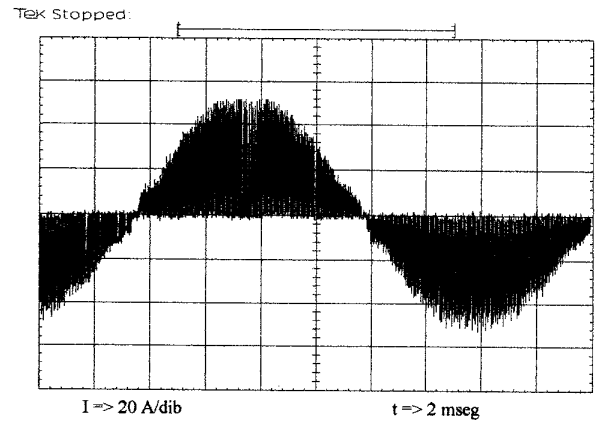


Fig. 21 Storage inductor current at network frequency.

8 REFERENCES:

- [1] A.R. Prasad, P.D. Ziogas, S. Manias "An active power factor correction technique for three-phase diode rectifiers ". PESC Records , 1989.
- [2] Clemens Niermann, "New rectifier circuits with low mains pollution and additional low cost inverter for energy recovery" EPE'89 pp 1131-1136