

A FAMILY OF ZVS-PWM ACTIVE-CLAMPING DC-TO-DC CONVERTERS: SYNTHESIS, ANALYSIS, AND EXPERIMENTATION

Cláudio M. C. Duarte^(*) and Ivo Barbi

Federal University of Santa Catarina
INEP - Power Electronics Institute
P.O. Box 5119
88040-970 - Florianópolis (SC) BRAZIL
Phone: 55 48 231 9204
FAX: 55 48 231 9770
E-mail: ivo@lamep.ufsc.br

ABSTRACT

This paper presents a technique to generate a complete family of two-switch pulse-width-modulated with active clamping DC/DC converters, featuring soft commutation of the semiconductors at zero-voltage (ZVS). The main purpose of this technique is to integrate these converters under a same theoretical principle to derive the topologies in a comprehensive form and generate new circuits.

All the converters have the advantage of soft commutation (ZVS) with minimum switch voltage stress due to the clamping action.

Besides operating at constant frequency and with reduced commutation losses, these converters have output characteristics similar to the PWM hard-switching counterpart, which means that there is no circulating reactive energy that would cause large conduction losses. Principle of operation, theoretical analysis, simulation and experimental results of one particular converter taken as an example, are provided in the paper.

1. INTRODUCTION

The two transformer active reset circuits presented in [1] and shown in Figure 1, were employed in a forward converter to operate over a wide input voltage range. These circuits recover transformer magnetizing and leakage inductance energies, reduce DC flux in the core, and minimize peak voltage on the power transistor. One of these circuits, Figure 1.b, was employed in a flyback converter [2] also to achieve soft switching. In [3], the other circuit, Figure 1.a, was employed in a forward converter with some modifications and the soft switching was obtained too. The circuit shown in Figure 1.a was used in [4] as a switched snubber

for switch and diode of high frequency PWM converters. In [5], the inter-relationships among two switch, soft-switched converters were analyzed and a generalization was searched by a generalized two-switched converter.

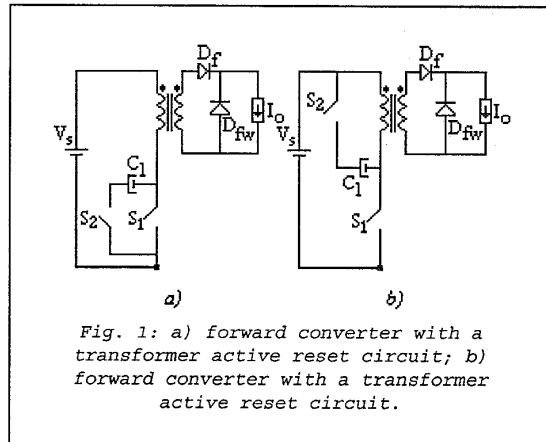


Fig. 1: a) forward converter with a transformer active reset circuit; b) forward converter with a transformer active reset circuit.

In this paper, the concept of fundamental ZVS-PWM cells was employed to generate a complete family of two-switch clamped mode ZVS-PWM DC-DC converters. This technique allows the generation, in a comprehensive form, of six basic family converters and from them, all isolated versions. The generation of the cells is described hereafter.

2. GENERATION OF A FAMILY OF CLAMPED MODE ZVS-PWM DC-TO-DC CONVERTERS

2.1. Generation of six fundamental clamped mode ZVS-PWM cells

Let us consider Figure 2, where a ZVS-PWM commutation cell is obtained. In the converter shown in Figure 2.b, the power transferred to the load is processed by a buck stage, while the clamping action is performed by a boost stage. For the same buck based power transfer, six clamped circuits, namely, buck, boost, buck-

^(*) UCPel - Catholic University of Pelotas-RS-BRAZIL
Ph.D. student at UFSC-INEP.

boost, ZETA, SEPIC, and Cuk, can be employed, and are shown in Figure 3. These circuits, when drawn in a different way, as shown in Figure 4, lead to the identification of the fundamental ZVS-PWM cells. The new cells are represented in Figure 5.

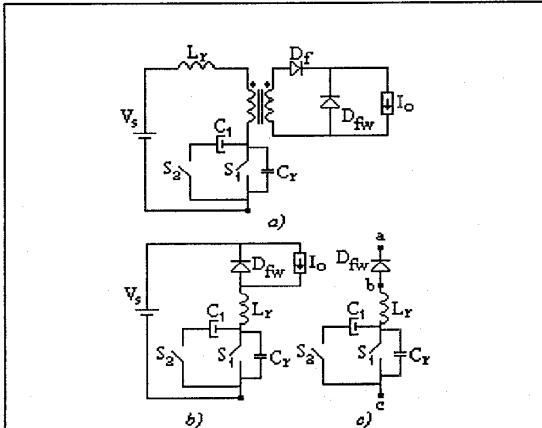


Fig. 2: a) clamped mode ZVS-PWM forward converter; b) clamping mode ZVS-PWM buck converter; c) the ZVS-PWM commutation cell taken from the buck converter.

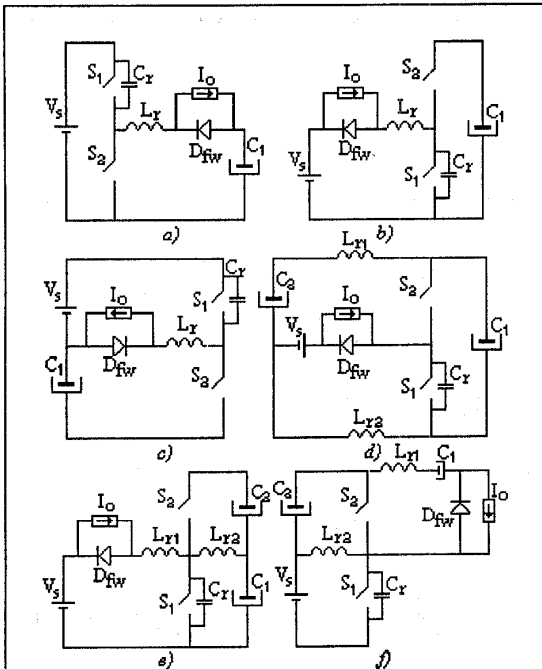


Fig. 3: Clamped mode ZVS-PWM Buck converters. a) Buck (buck); b) Buck (boost); c) Buck (buck-boost); d) Buck (cuk); e) Buck (SEPIC); f) Buck (ZETA).

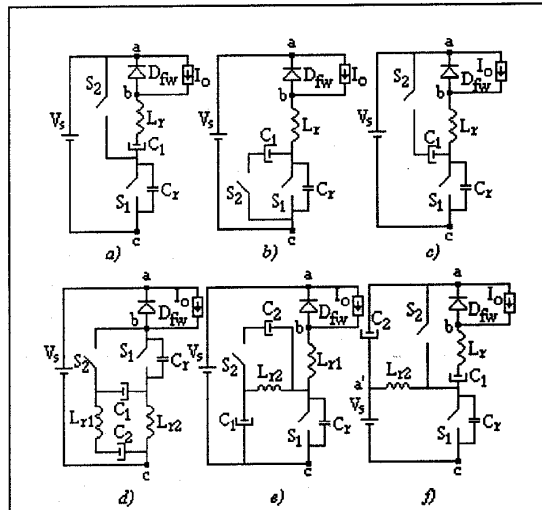


Fig. 4: Clamped mode ZVS-PWM Buck converters. a) Buck (buck); b) Buck (boost); c) Buck (buck-boost); d) Buck (cuk); e) Buck (SEPIC); f) Buck (ZETA).

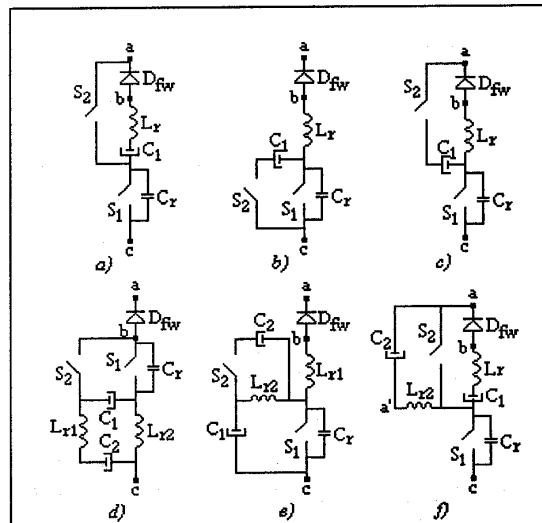


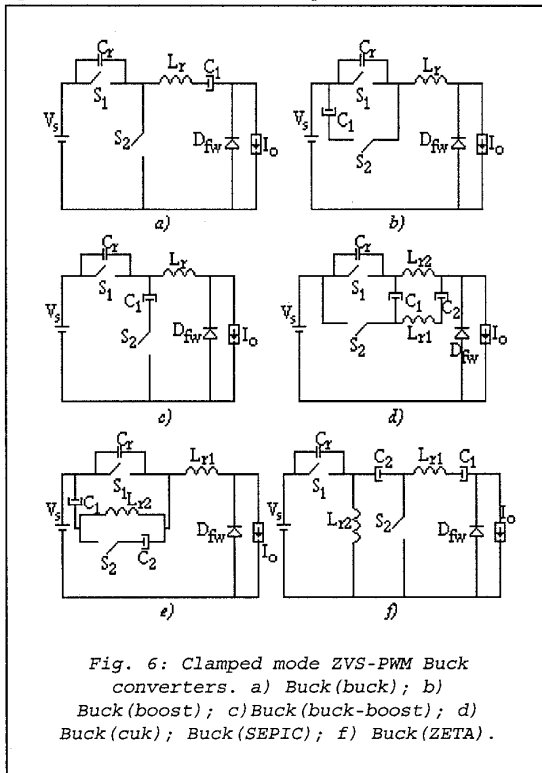
Fig. 5: Fundamental ZVS-PWM cells. a) clamping action buck; b) clamping action boost; c) clamping action buck-boost; d) clamping action cuk; e) clamping action SEPIC; f) clamping action ZETA.

2.2. Generation of the family of new converters

Each of the commutation cells identified above, by a proper connection of voltage and current sources, generate six non-isolated circuits. Therefore, using this systematic approach, 36 topologies are obtained, divided in six groups according to their power transfer principle. Due to lack of space, only the Buck converter is

taken as an example. In order, to help the understanding of this approach, the same group composed by the six buck converters is shown in Figure 6. In this Figure the circuits are drawn in a more usual way, making the identification of the Buck converter easier.

In the following section, the clamped mode ZVS-PWM buck converter with the clamping action processed by a Boost stage, Figures 3.b, 4.b, and 6.b, is taken as an example to illustrate the operation of this family.



3. OPERATION AND ANALYSIS OF THE CLAMPED MODE ZVS-PWM BUCK CONVERTER WITH THE CLAMPING ACTION BOOST.

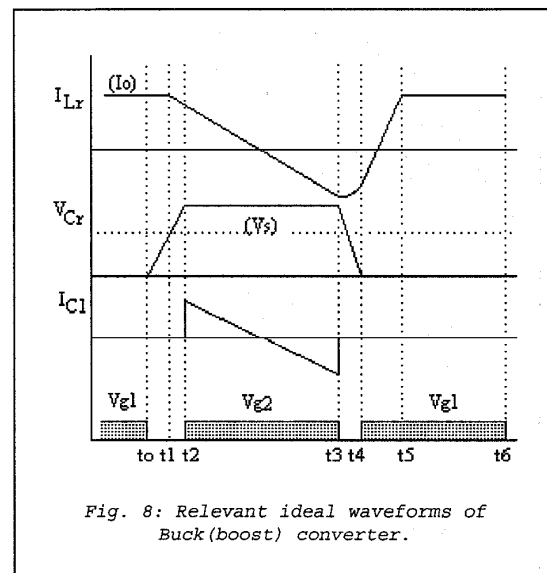
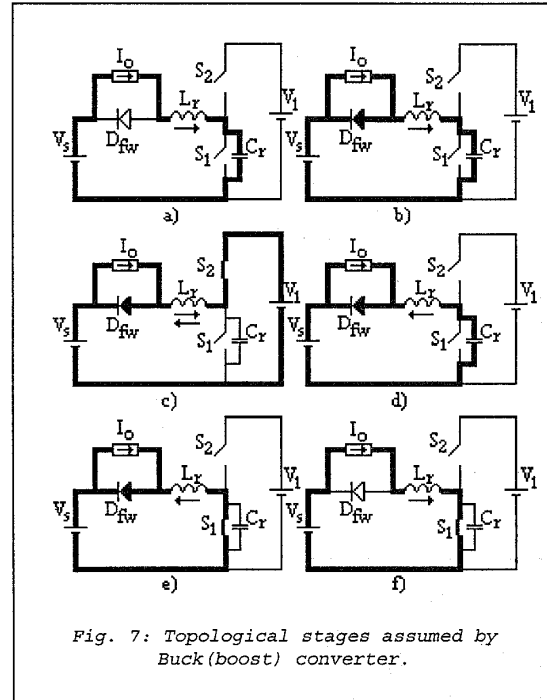
This converter differs from a conventional Buck PWM converter by an additional auxiliary switch (S_2), a resonant inductor (L_r), a resonant capacitor (C_r), which includes the output capacitance of the power switch, and a clamping capacitor (C_1). S_1 is the main switch, which is responsible for the power transferred to the load.

3.1. Operation of the Buck(boost) converter

To simplify the analysis, the output filter inductance is assumed large enough to be considered as a current source

(I_0). The capacitor (C_1) is selected to have a large capacitance so that the voltage V_1 across the capacitor C_1 could be considered as a constant one.

The six topological stages and key waveforms of the Buck(boost) converter to one switching cycle, are shown in Figure 7 and 8. In those Figures it can be seen that the two switches are switched in a complementary way. The main switch S_1 is turned off at $t=t_0$, when the switching period starts.



STAGE 1: $[t_0, t_1]$, Figure 7.a

Prior to t_0 , the main switch (S_1) is on and the auxiliary switch is off. When S_1 is turned off at t_0 , the capacitor C_r is linearly charged, by I_0 , to V_s . Due to the presence of C_r , S_1 is turned off with no switching loss.

The equations that describe this stage are:

$$I_{Lr}(t) = I_0 \quad (1)$$

$$V_{Cr}(t) = \frac{I_0}{C_r} t \quad (2)$$

This stage ends when $V_{Cr}(t) = V_s$. Thus,

$$\Delta t_1 = \frac{C_r}{I_0} V_s \quad (3)$$

STAGE 2: $[t_1, t_2]$, Figure 7.b

When V_{Cr} reaches V_s , the free-wheeling diode (D_{fw}) starts conducting, then the current I_{Lr} and V_{Cr} involve in a resonant way, and V_{Cr} rises from V_s up to V_1 . After that, the voltages are clamped. The behavior of this stage is described by:

$$I_{Lr}(t) = I_0 \cos \omega_0 t \quad (4)$$

$$V_{Cr}(t) = V_s + Z_0 I_0 \sin \omega_0 t \quad (5)$$

Where:

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad (6)$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \quad (7)$$

This stage ends when $V_{Cr}(t) = V_1$, hence:

$$\Delta t_2 = \frac{1}{\omega_0} \sin^{-1} \left(\frac{V_1 - V_s}{Z_0 I_0} \right) \quad (8)$$

STAGE 3: $[t_2, t_3]$, Figure 7.c

As $V_{Cr}(t) = V_1$, the voltage across S_2 is zero, thus S_2 turns on with no losses (ZVS). The L_r current ramps down until it reaches zero, when it changes its direction and rises again.

The equations below describe the behavior of this stage. Thus:

$$I_{Lr}(t) = \frac{(V_s - V_1)}{L_r} t + I_0 \sqrt{1 - \left(\frac{V_1 - V_s}{Z_0 I_0} \right)^2} \quad (9)$$

$$V_{Cr}(t) = V_1 \quad (10)$$

This stage ends when S_2 is turned off at t_3 , and:

$$\Delta t_3 = DT_s - \Delta t_4 - \Delta t_2 - \Delta t_1 \quad (11)$$

Where: D : duty cycle;
 T_s : switching period.

STAGE 4: $[t_3, t_4]$, Figure 7.d

The voltage across C_r falls due to the resonance between L_r and C_r . This stage is described by:

$$I_{Lr}(t) = \frac{(V_1 - V_s)}{Z_0} \sin \omega_0 t + I_3 \cos \omega_0 t \quad (12)$$

$$V_{Cr}(t) = V_s + (V_1 - V_s) \cos \omega_0 t - Z_0 I_3 \sin \omega_0 t \quad (13)$$

This stage finishes when V_{Cr} reaches zero at t_4 . Then:

$$\omega_0 \Delta t_4 = \tan^{-1} \left[\frac{-Z_0 I_3}{V_1 - V_s} \right] + \cos^{-1} \left[\frac{-V_s}{\sqrt{(Z_0 I_3)^2 + (V_1 - V_s)^2}} \right] \quad (14)$$

STAGE 5: $[t_4, t_5]$, Figure 7.e

In this stage S_1 is turned on with no switching losses (ZVS), because V_{Cr} became null. The current through I_{Lr} changes its polarity and ramps up to reaches I_0 .

The behavior of this stage is described by:

$$I_{Lr}(t) = \frac{V_s}{L_r} t + I_4 \quad (15)$$

$$V_{Cr}(t) = 0 \quad (16)$$

This stage ends when $I_{Lr}(t) = I_0$. Thus:

$$\Delta t_5 = L_r \left(\frac{I_0 - I_4}{V_s} \right) \quad (17)$$

STAGE 6: $[t_5, t_6]$, Figure 7.f

At $t = t_5$, The diode D_{fw} becomes reversibly biased and power is transferred to the load through main switch (S_1). The equations that describe this stage are:

$$I_{Lr}(t) = I_0 \quad (18)$$

$$V_{Cr}(t) = 0 \quad (19)$$

This stage ends when S_1 is turned off at the end of the switching cycle. Thus:

$$\Delta t_6 = DT_s \quad (20)$$

3.2.Relevant Analysis

As the time intervals Δt_1 , Δt_2 and Δt_3 are very short, in relation to the switching cycle, they will not be considered in this analysis. Thus, let us consider the waveform shown in Figure 9. The power that flows in the clamping capacitor must be zero in a switching cycle, for the operation to be steady. The voltage across C_1 is constant, so its average current must be zero. Thus:

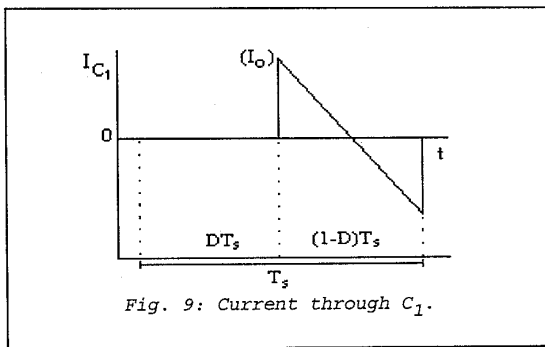


Fig. 9: Current through C_1 .

$$\int_0^{(1-D)T_s} \left[\frac{(V_1 - V_s)}{L_r} t + I_0 \right] dt = 0 \quad (21)$$

Then,

$$\beta = 1 + \frac{2}{(1-D)} L_n \quad (22)$$

Where:

$$\beta = \frac{V_1}{V_s} \quad (23)$$

$$L_n = L_r \frac{I_0}{V_s T_s} \quad (24)$$

The DC voltage clamping ratio given by (22), is graphically represented in Figure 10.

The average voltage across S_1 is given by (25).

$$V_{S1_{avg}} = (1-D)V_1 \quad (25)$$

Then, the output voltage is given by (26).

$$V_0 = V_s - (1-D)V_1 \quad (26)$$

Thus,

$$q = \frac{V_0}{V_s} = 1 - (1-D)\beta \quad (27)$$

or,

$$q = D - 2L_n \quad (28)$$

Where q is the DC voltage conversion ratio and is shown in Figure 11.

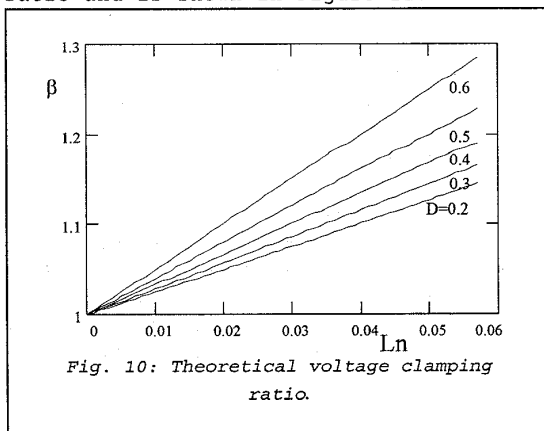


Fig. 10: Theoretical voltage clamping ratio.

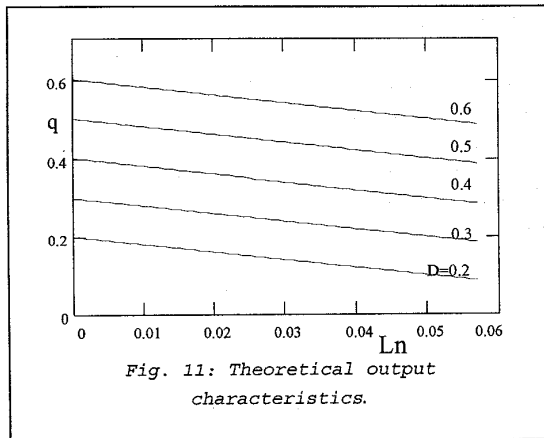


Fig. 11: Theoretical output characteristics.

Due to the capacitance C_r , S_1 and S_2 are turned off with no losses, in a ZVS way. However, S_1 and S_2 will turn on with no losses, only if there is enough energy stored in L_r to achieve soft commutation. At t_1 , it is necessary to charge C_r from V_s to V_1 . At t_3 , it is necessary to discharge C_r from V_1 to zero. The latter is more difficult because it needs more energy. Thus, if enough energy is guaranteed to achieve soft commutation for S_1 , S_2 will achieve soft commutation too.

Thus, from energy relationships for L_r and C_r , at $t = t_3$, we have:

$$\frac{Z_0 I_0}{V_1} \geq 1 \quad (29)$$

and,

$$L_n \geq \frac{(1-D)}{(1-D)\omega_0 T_s - 2} \quad (30)$$

4. RELEVANT ANALYSIS RESULTING FROM THE ENTIRE FAMILIES OF CONVERTERS

All converters were analyzed and it was possible to take some conclusions by comparing their performances. Shown below is the voltage clamping ratio and the DC voltage conversion ratio, for all proposal buck converters.

a. Buck (buck)

$$\beta = \frac{2L_n}{2L_n + (1-D)^2} \quad q = D - \frac{2L_n}{2L_n + (1-D)^2}$$

b. Buck (boost)

$$\beta = 1 + \frac{2L_n}{(1-D)} \quad q = D - 2L_n$$

c. Buck (buck-boost)

$$\beta = \frac{2L_n}{(1-D)} \quad q = D - 2L_n$$

d. Buck (Cuk)

$$\beta = 1 + \frac{2L_n}{(1-D)} \quad q = D - 2L_n$$

e. Buck (SEPIC)

$$\beta = D \left[1 + \frac{2L_n}{(1-D)} \right] \quad q = D - 2L_n$$

f. Buck (ZETA)

$$\beta = \frac{2L_n}{[2(1-D)L_n + (1-D)^2]} \quad q = \frac{1}{-(1-D)} \left[D - \frac{2L_n}{2L_n + (1-D)} \right]$$

The converters from (b) to (e) present the same external characteristics, but with different voltages across the switches. Through the analysis it was proved that the converters (a) and (f), presented lower voltage across the switches, but higher current stresses.

5. DESIGN EXAMPLE AND SIMULATION

The input and output data are as follows:

$V_{in}=150V$ (input voltage); $V_0=50V$ (output voltage); $P_{out}=500W$ and $f_s=100kHz$.

With this data and the equations obtained by analysis, we have:

$$q = 0.333; L_n = 0.033; D = 0.4; \beta = 1.111$$

$$L_x = 5\mu H \quad C_x = 1730pF \quad C_1 = 470\mu F$$

The output inductor filter (L_f) and capacitor (C_f) are given by

$$L_f = 160\mu H \quad C_f = 440\mu F$$

Figure 12 shows the implemented circuit of the new Buck ZVS-PWM converter.

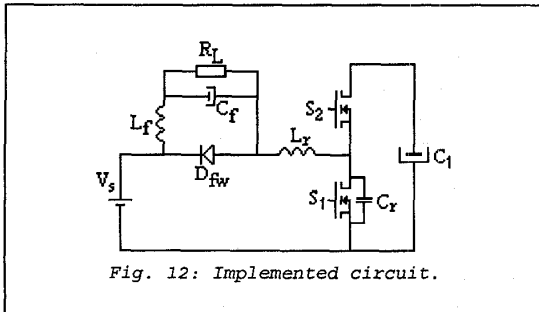


Fig. 12: Implemented circuit.

Figure 13 shows the main waveforms of the converter from simulation.

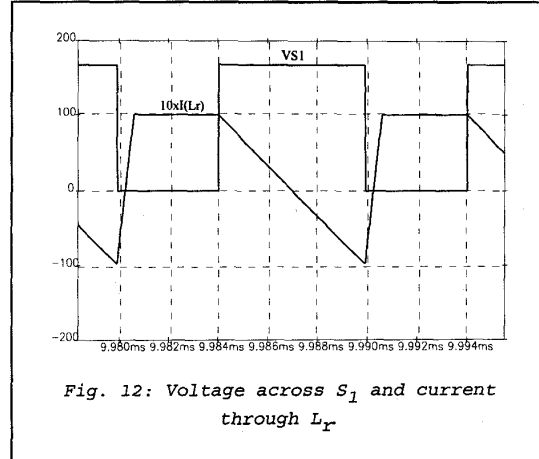


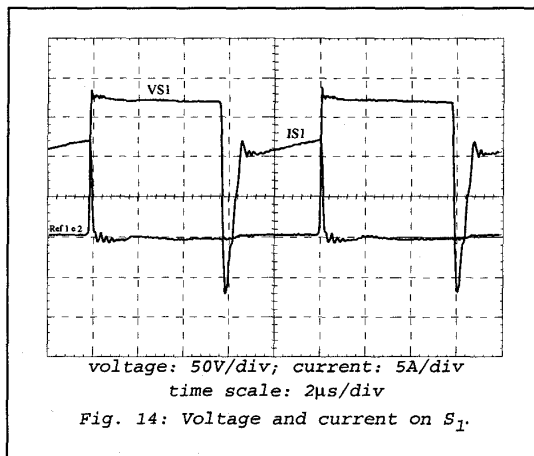
Fig. 12: Voltage across S_1 and current through L_x

6. EXPERIMENTAL RESULTS

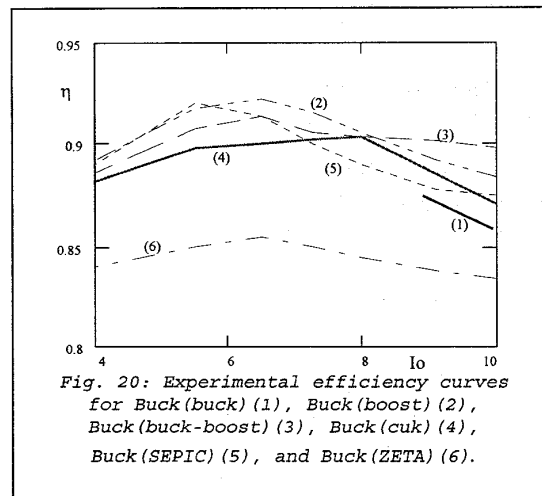
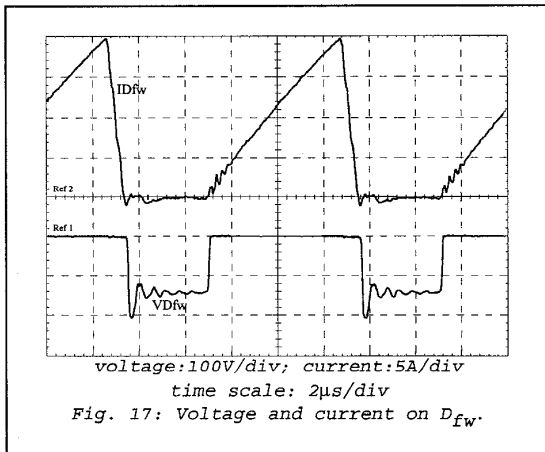
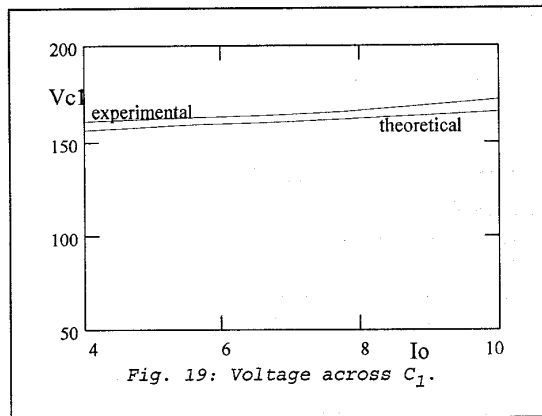
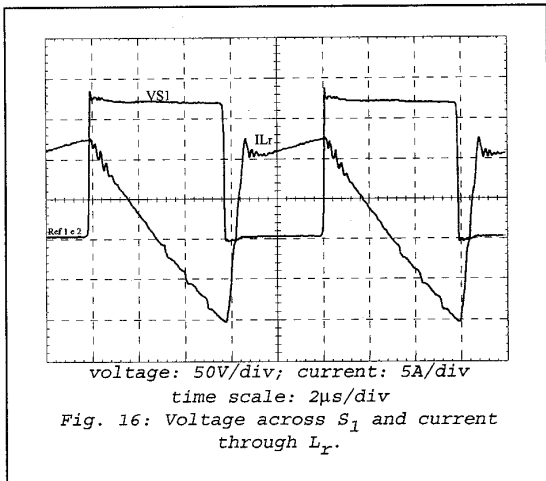
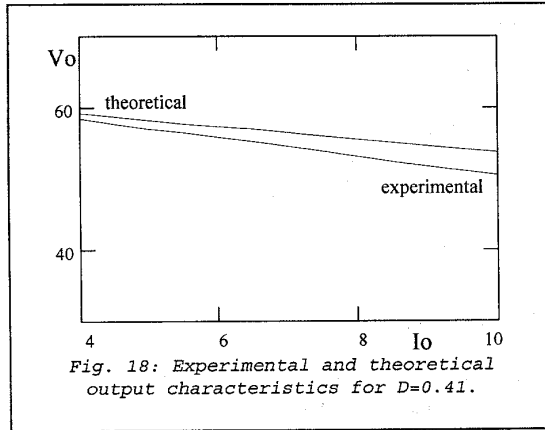
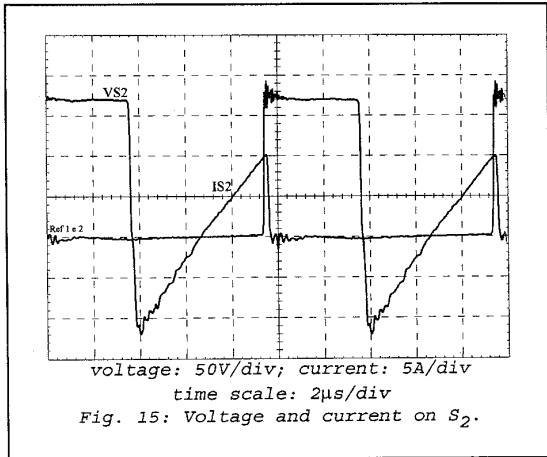
The specifications and the values of the parameters are the following:

- constant voltage source: $V_{in}=150V$;
- switches S_1 and S_2 : Power MOSFET's APT5025;
- diode D_{fw} : APT60D60;
- resonant capacitor C_x : 1000pF/1.6kV;
- clamping capacitor C_1 : 470uF/250V;
- output filter capacitor C_f : 2x220uF/63V;
- resonant inductor L_x : 5,0uH, core(E-30/7);
- output filter inductor L_f : 160uH, core(E-42/15).

The experimentally obtained relevant waveforms are shown in Figures 14, 15,16, 17, 18, and 19.



voltage: 50V/div; current: 5A/div
time scale: 2us/div
Fig. 14: Voltage and current on S_1 .



Experimental and theoretical curves of output characteristics and voltage across C_1 are shown in Figures 18 and 19.

Figure 20 shows the experimental efficiency curves for the six Buck converters. From this Figure it is possible to conclude that the Buck(ZETA) converter presents less efficiency. In fact, its conduction losses are the greatest, but its load range with soft-commutation is the largest. It presents

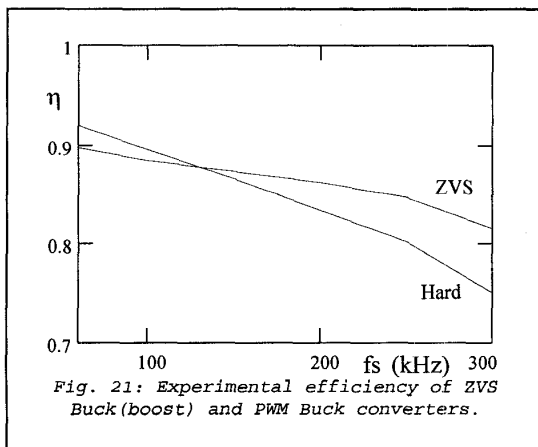
soft-commutation from non-load to full load.

The experimental results are in agreement with the results predicted theoretically and demonstrate that zero-voltage-switching is achieved at constant frequency for both active switches (S_1 and S_2).

7. COMPARISON BETWEEN THE CLAMPED MODE ZVS-PWM BUCK CONVERTER WITH THE CLAMPING ACTION BOOST, AND HARD-SWITCHING-PWM BUCK CONVERTER

It is well known that to achieve soft-commutation, the conduction losses in a power converter are increased. One natural concern is to identify the operation frequency for which the ZVS-PWM converter is more efficient than its hard-switching counterpart. To determine this limit frequency theoretically is not a simple task. Therefore, in this paper this frequency has been determined experimentally, as described hereafter. The experimental results of efficiency, for different frequencies, for the clamped mode ZVS-PWM with the clamping action boost and hard-switching PWM Buck converters, employing the same switches and gate drive circuit, with identical input and output characteristics, are shown in Figure 21.

With the results shown in Figure 21, we demonstrate that despite this new family of converters employing an auxiliary switch, for frequencies greater than 120 kHz, their efficiency is greater than their hard-switching PWM counterparts.



8. CONCLUSION

This paper presented a technique to generate a complete family of ZVS-PWM Active-Clamping DC-to-DC Converters. From this technique it was possible to generate 36 non-isolated topologies, where most of them are new. Those topologies were derived in a comprehensive form, and one Buck converter was analyzed as an example. Theoretical studies and experimental results, allow us to draw the following conclusions:

- soft-commutation (ZVS) is achieved for the active switches;
- the converters are regulated by the conventional PWM technique, at constant frequency;
- greater efficiency than the conventional hard-switching DC-DC converters at high frequencies was achieved.

9. REFERENCES

- [1] B. Carsten, "Design Techniques for Transformers Active Reset Circuits at High Frequencies and Power Levels", HFPC 1990, pp. 235-246.
- [2] R. Watson, F.C. Lee, and G.C. Hua, "Utilization of an Active-Clamp Circuit to Achieve Soft Switching in Flyback Converters", PESC 1994, pp. 909-916.
- [3] I.D. Jitaru, "Constant Frequency, Forward Converter with Resonant Transition", HFPC 1991, pp. 282-292.
- [4] K. Harada and H. Sakamoto, "Switched Snubber for High Frequency Switching", PESC 1990, pp.181-188.
- [5] P.C. Heng and R. Oruganti, "Family of Two-Switch Soft-Switched Asymmetrical PWM DC/DC Converters" PESC 1994, pp. 85-94.
- [6] P. Imbertson and N. Mohan, "Asymmetrical Duty Cycle Zero Switching Loss in PWM Circuits with no Conduction Loss Penalty", IEEE IAS Annual Meeting 1991, pp. 1061-1066.