

A NEW ZVS SEMI-RESONANT HIGH POWER FACTOR RECTIFIER WITH REDUCED CONDUCTION LOSSES

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Abstract - This paper presents a novel single-phase unity power factor rectifier, which features Critical Conduction Mode and Zero Voltage Switching. The reduced conduction losses are achieved by the employment of a single converter, instead of the typical configuration composed of a front end rectifier followed by a boost converter. Theoretical analysis, a design example and experimental results of a 300 W converter with 127 V_{rms} input voltage and 400 V_{DC} output voltage are presented.

I. INTRODUCTION

The converter usually employed for single-phase power factor correction consists of a front end diode rectifier bridge followed by a boost converter. This converter, however, presents conduction and commutation losses, which will contribute for the reduction in the efficiency of the converter. The commutation losses occur due to the hard switching of power semiconductors, and the conduction losses are representative because there are always three semiconductors in the current flow path.

The reduction of the commutation losses can be achieved by different techniques, which can employ ZVS or ZCS [1], [2], [3]. With these converters, the efficiency is improved, but the conduction losses are significant.

The converter presented in reference [4] presents much lower conduction losses, due to the fact that there are always two semiconductors in the current flow path. However the commutation losses problem is not solved.

In order to improve the efficiency even more, references [5] and [6] proposed power factor correction rectifiers with soft-commutation and reduced conduction losses. Due to complexity and cost, these converters are suitable for high power single phase applications, once they employ the continuous conduction mode to achieve high power factor.

For low-power single phase applications, it can be employed the boost converter with the discontinuous conduction mode using the voltage follower technique [7]. This technique, however, naturally presents hard-commutation and input current distortion.

Another solution for low-power single phase applications is the boost converter in critical conduction mode, which features high power factor with simplicity and low cost [8]. However, this converter presents commutation losses and expressive conduction losses.

In order to obtain high power factor and high efficiency, a new converter employing a ZVS semi-resonant boost converter with reduced conduction losses is proposed in this paper.

II - THE PROPOSED CONVERTER

The main topology is depicted in Fig. 1. This converter will operate as two boost converters, one for each half line cycle. When the input current is positive, the body diode of MOSFET M₂ or MOSFET M₂ itself, depending on the MOSFET's channel resistance, will conduct, while MOSFET M₁ and diode D₁ will perform the boost function with power factor correction in critical conduction mode. When the input current is in the reverse direction, MOSFET M₂ and diode D₂ will perform the boost function with power factor correction in critical conduction mode, while the body diode of MOSFET M₁ or MOSFET M₁ will conduct. The resonant capacitors C_{r1} and C_{r2} along with the input inductor L_{in}, will be responsible for the Zero-Voltage Switching of M₁ and M₂ employing the semi-resonance.

The critical conduction mode will ensure near unity power factor with variable switching frequency.

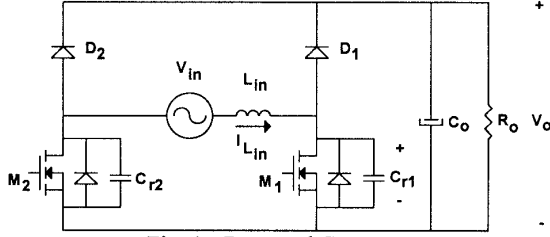


Fig. 1 - Proposed Converter.

III - PRINCIPLE OF OPERATION

In order to analyze the commutation process, it is considered that the minimum switching frequency is much higher than the AC mains frequency. Thus, the sinusoidal input voltage can be considered constant for each period of operation. The output voltage can be represented by a constant DC voltage source. In the following analysis, the commutation process will be analyzed for the peak of the sinusoidal input voltage (V_{inp}). The MOSFET's M_1 and M_2 will present a protection circuit [9], which will prevent them from conducting when their drain-to-source voltage is greater than zero and the gate signal is high. This protection circuit, based on the dual-thyristor principle, will ensure the ZVS commutation.

1st Stage (t_0, t_1) - Linear stage

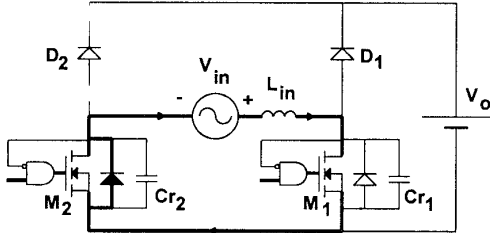


Fig. 2 - Linear Stage.

At the beginning of this stage (t_0), the current through L_{in} is null and the voltage across C_{r1} and C_{r2} are null. The MOSFET's M_1 and M_2 are turned on and the input current flows through them. The input current will flow through the body diode of MOSFET M_2 or through the MOSFET's channel, depending of its on-resistance.

$$V_{Cr1}(t) = 0 \quad (1)$$

$$I_{Lin}(t) = \frac{V_{inp}}{L_{in}} \cdot t \quad (2)$$

In order to simplify the analysis, the voltage V_{Cr1} and the current I_{Lin} can be normalized.

$$\bar{V}_{Cr1}(t) = 0 \quad (3)$$

$$\bar{I}_{Lin}(t) = \frac{\omega_o \cdot t}{\beta} \quad (4)$$

Where:

$$\beta = \frac{V_o}{V_{inp}} \quad (5)$$

$$\bar{V}_{Cr1}(t) = \frac{V_{Cr1}(t)}{V_o} \quad (6) \quad \bar{I}_{Lin}(t) = \sqrt{\frac{L_{in}}{C_{r1}}} \cdot \frac{I_{Lin}}{V_o} \quad (7)$$

$$\omega_o = \frac{1}{\sqrt{L_{in} \cdot C_{r1}}} \quad (8) \quad Z_o = \sqrt{\frac{L_{in}}{C_{r1}}} \quad (9)$$

In order to obtain a high power factor, the on-time (t_{on}) of MOSFET M_1 must be maintained constant during all the AC mains period. Thus, the peak of the current through L_{in} (I_p) will follow the sinusoidal shape of the input voltage.

2nd Stage(t_1, t_2) - Resonant Stage

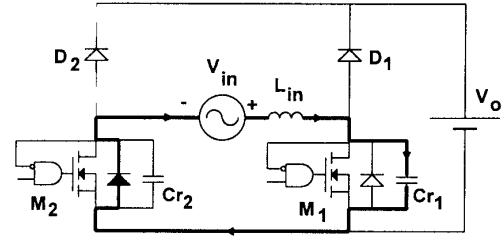


Fig. 3 - Resonant stage.

At time t_1 MOSFET M_1 and M_2 are turned off. The input current flows through C_{r1} and begins to charge it in a resonant way.

$$V_{Cr1}(t) = V_{inp} \cdot (1 - \cos \omega_o \cdot t) + Z_o \cdot I_p \cdot \sin(\omega_o \cdot t) \quad (10)$$

$$I_{Lin}(t) = \frac{V_{inp}}{Z_o} \cdot \sin \omega_o \cdot t + I_p \cdot \cos \omega_o \cdot t \quad (11)$$

Normalizing (10) and (11) :

$$\bar{V}_{Cr1}(t) = \frac{1}{\beta} \cdot (1 - \cos \omega_o \cdot t) + \frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o} \cdot \sin \omega_o \cdot t \quad (12)$$

$$\bar{I}_{Lin}(t) = \frac{1}{\beta} \cdot \sin \omega_o \cdot t + \frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o} \cdot \cos \omega_o \cdot t \quad (13)$$

This stage finishes when $V_{Cr1}(t) = V_o$, or $\bar{V}_{Cr1}(t) = 1$.

3rd Stage (t_2, t_3) - Linear stage

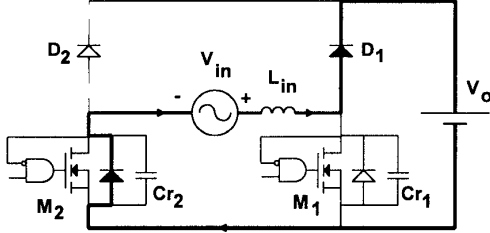


Fig. 4 - Linear stage.

At instant t_2 , the voltage $V_{Cr1}(t)$ is equal to V_o . The diode D_1 begins to conduct the input current. The input inductor begins to demagnetize linearly, and the current begins to fall at the same rate.

$$V_{Cr1}(t) = V_o \quad (14)$$

$$I_{Lin}(t) = I_{Lin}(t_2) - \frac{(V_o - V_{in,p}) \cdot t}{L_{in}} \quad (15)$$

Normalizing (14) and (15):

$$\bar{V}_{Cr1}(t) = 1 \quad (16)$$

$$\bar{I}_{Lin}(t) = \sqrt{\left(\frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o}\right)^2 - 1} + \frac{2}{\beta} - \frac{1}{\beta} (\beta - 1) \cdot \omega_o \cdot t \quad (17)$$

This stage finishes when the input inductor current becomes null.

4th Stage (t_3, t_4) - Resonant Stage

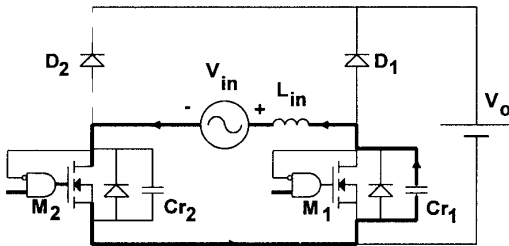


Fig. 5 - Resonant Stage

At instant t_3 the input inductor current becomes null and diode D_1 turns off. At this time, the control circuit will apply a gate signal to the drive circuits of both MOSFET's. However, only MOSFET M_2 begins to conduct immediately, because the dual-thyristor circuit prevents MOSFET M_1 to conduct while its drain to source voltage does not reach zero. The current I_{Lin} inverts its sense and a resonant stage makes the discharge of capacitor C_{r1} .

$$V_{Cr1}(t) = (V_o - V_{in,p}) \cdot \cos \omega_o t + V_{in,p} \quad (18)$$

$$I_{Lin}(t) = \frac{(V_{in,p} - V_o)}{Z_o} \cdot \sin \omega_o t \quad (19)$$

Normalizing:

$$\bar{V}_{Cr1}(t) = \frac{1}{\beta} [(\beta - 1) \cdot \cos \omega_o \cdot t + 1] \quad (20)$$

$$\bar{I}_{Lin}(t) = \frac{1}{\beta} (1 - \beta) \cdot \sin \omega_o \cdot t \quad (21)$$

This stage finishes when the voltage across C_{r1} becomes null.

The output voltage must be greater than the double of the input voltage in order to ensure the complete discharge of C_{r1} and guarantee the ZVS.

5th Stage (t_4, t_5) - Linear Stage

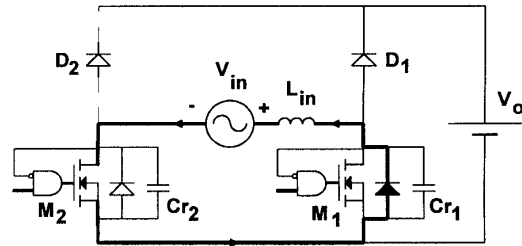


Fig. 6 - Linear Stage.

When the voltage across C_{r1} becomes null at t_4 , the body diode of MOSFET M_1 begins to conduct the input inductor current. The current through L_{in} begins to increase linearly.

$$I_{Lin}(t) = -\frac{V_{in,p}}{Z_o} \cdot \sqrt{\frac{V_o}{V_{in,p}} \cdot \left(\frac{V_o}{V_{in,p}} - 2\right)} + \frac{V_{in,p}}{L_r} \cdot t \quad (22)$$

$$V_{Cr1}(t) = 0 \quad (23)$$

Normalizing:

$$\bar{I}_{Lin}(t) = -\sqrt{\frac{\beta - 2}{\beta}} + \frac{1}{\beta} \cdot \omega_o \cdot t \quad (24)$$

$$\bar{V}_{Cr1}(t) = 0 \quad (25)$$

This stage finishes when $I_{Lin}=0$. During this stage the MOSFET M_1 can be turned on. Thus, the MOSFET M_1 will commutate under ZVS.

Symmetrical operation stages will occur when the input voltage has a reverse polarity.

The input inductor current and the voltage across C_{r1} for one operation period is shown in Fig. 7. This

figure is normalized by the peak of the input inductor current at the peak of the sinusoidal input voltage.

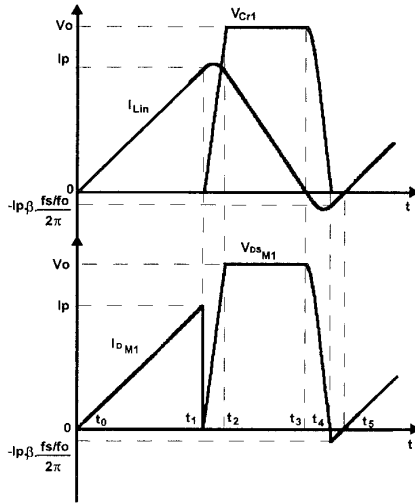


Fig. 7 - Main waveforms.

IV - THE BOOST CONVERTER IN CRITICAL CONDUCTION MODE AND THE POWER FACTOR CORRECTION

The boost converter operating in critical conduction mode can achieve a high power factor with constant on-time of MOSFET's M₁ and M₂. Thus, the peak current through L_{in} will naturally follow the sinusoidal shape of the input voltage.

As the converter will operate in critical conduction mode, the switching frequency will be variable along the cycle of the input voltage. The switching frequency variation along half cycle of the input voltage and normalized as function of the minimum switching frequency is defined by expression (26) and depicted in Fig. 8.

$$\bar{f}_s = \frac{f_s(t)}{f_{s\min}} = \frac{\beta - \sin(\omega t)}{\beta - 1} \quad (26)$$

Where : $f_{s\min}$ - minimum switching frequency

The power factor obtained for this type of converter considering that an appropriate filtering of the input inductor current is made, is defined by expression (27).

$$P.F. = \frac{1}{\sqrt{\pi}} \cdot \frac{\text{fr} \cdot \beta \cdot (\pi - 4 \cdot \beta) + \pi \cdot (\beta - 1)}{\sqrt{\text{fr} \cdot (-8 \cdot \beta^3 + \pi \cdot \beta^2 \cdot \text{fr} - 8 \cdot \beta^3 \cdot \text{fr} + 2 \cdot \pi \cdot \beta^4 \cdot \text{fr} + 2 \cdot \pi \cdot \beta^2 - 2 \cdot \pi \cdot \beta + 8 \cdot \beta^2) + \pi \cdot (\beta - 1)^2}} \quad (27)$$

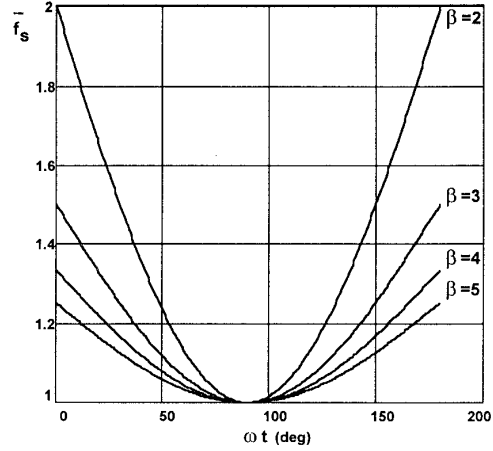


Fig. 8 - Switching frequency variation along half line cycle.

The power factor as function of the gain β for some relations of $f_{s\min}/f_o$ is shown in Fig. 9. It can be noticed that the power factor is very high for all the situations.

The voltage ratio $\beta = V_o/V_{inp}$ as function of \bar{I}_o , t_{on} and f_o is defined by expression (29).

$$\beta = \frac{2 \cdot \pi}{5} \cdot t_{on} \cdot f_o \cdot \left[\frac{4}{\pi} + \frac{2}{t_{on} \cdot f_o \cdot \pi^2} - \bar{I}_o \right] \quad (29)$$

Where :

$$\bar{I}_o = \frac{I_o}{I_{o\text{nom}}} \quad (30)$$

$I_{o\text{nom}}$ - Output Current for rated power.

The output characteristics of this converter is shown in Fig. 10. It can be observed the current source characteristic of the output, once it is indirectly imposed by the input current.

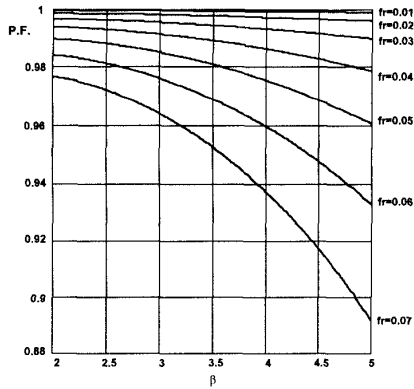


Fig. 9 - Power factor variation as function of β .

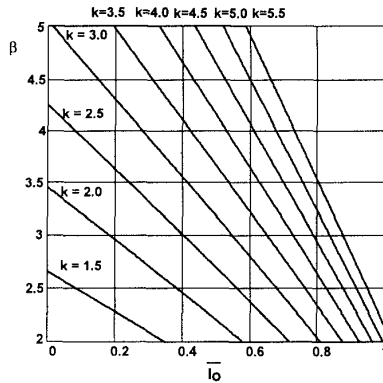


Fig. 10 - Output characteristics.

V - DESIGN PROCEDURE AND EXAMPLE

A simplified design procedure and example is described in this section as follows:

1. Input Data

$$\begin{aligned} V_o &= 400 \text{ V} & V_{in} &= 127 \text{ Vrms} \\ P_o &= 300 \text{ W} & f_{s\min} &= 60 \text{ kHz} & f_o &= 500 \text{ kHz} \end{aligned}$$

2. Determination of β and t_{on} :

$$\beta = \frac{V_o}{V_{in\ p}} = \frac{400}{179.6} = 2.23$$

$$t_{on} = \frac{\beta - 1}{\beta \cdot f_{s\min}} = 9.18 \mu\text{s}$$

3. Determination of the input inductance L_{in} .

$$L_{in} = \frac{V_o^2 \cdot (\beta - 1)}{4 \cdot \beta^3 \cdot P_o \cdot f_{s\min}} = \frac{400^2 \cdot (2.227 - 1)}{4 \cdot 2.227^3 \cdot 300 \cdot 60 \cdot 10^3} = 246.85 \mu\text{H}$$

4. Determination of the maximum switching frequency

$$f_{s\max} = \frac{\beta \cdot f_{s\min}}{\beta - 1} = 108.9 \text{ kHz}$$

5. Determination of the resonant capacitor

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{in} \cdot C_{r1}}} \quad C_{r1} = C_{r2} = \frac{1}{4 \cdot \pi^2 \cdot f_o^2 \cdot L_{in}} = 410 \text{ pF}$$

6. Peak input inductor current

$$I_p = \frac{V_p}{L_{in}} \cdot t_{on} = \frac{179.6 \times 9.18 \times 10^{-6}}{246.85 \times 10^{-6}} = 6.68 \text{ A}$$

7. Expected power factor

Examining Fig. 9, it can be noticed that the expected power factor will be better than 0.995. By substituting the values of f_r and β in expression (27), the expected power factor will be 0.998.

VI - EXPERIMENTAL RESULTS

In order to experimentally verify the principle of operation and the theoretical analysis, a 300W, Semi-Resonant ZVS high power factor converter has been implemented in laboratory. The Quasi-Resonant ZCS high power factor converter has been implemented in laboratory using Unitrode's critical conduction mode IC, UC3852 [8]. The prototype was tested with an input voltage of 127 V_{rms} and an output voltage of 400 V_{DC}. The complete diagram of the prototype is shown in Fig. 11. The dual-thyristor principle [9] is employed to ensure the Zero-Voltage-Switching of the MOSFET's. The power components specification is as follows:

- M₁, M₂ - APT5025
- D₁-D₂ - MUR 460
- L_{in} - 270 μ H - 46 turns (6 x 25 AWG) on EE-42/15 core (gap = 1.9 mm).
- L_f - 1.5 mH - 99 turns (19 AWG) on EE-42/15 core (gap = 1.5 mm).
- C_f - 1 μ F/250 V (polypropylene)
- C_o - 680 μ F/500 V

In Fig. 12 it is shown the input voltage and the filtered input current. The power factor obtained was 0.997 with a THD of 8.2 % in the input current. The obtained efficiency for full load was 96.7%. In Fig. 13 it is shown the efficiency comparison of the ZVS semi-resonant converter in critical conduction mode and the hard-switched converter in critical conduction mode. It can be noticed the improvement in the efficiency due to the semi-resonance. The hard-switched converter presents a 50% increase on the losses (15W) in comparison to the Semi-Resonant converter (10W) for full load.

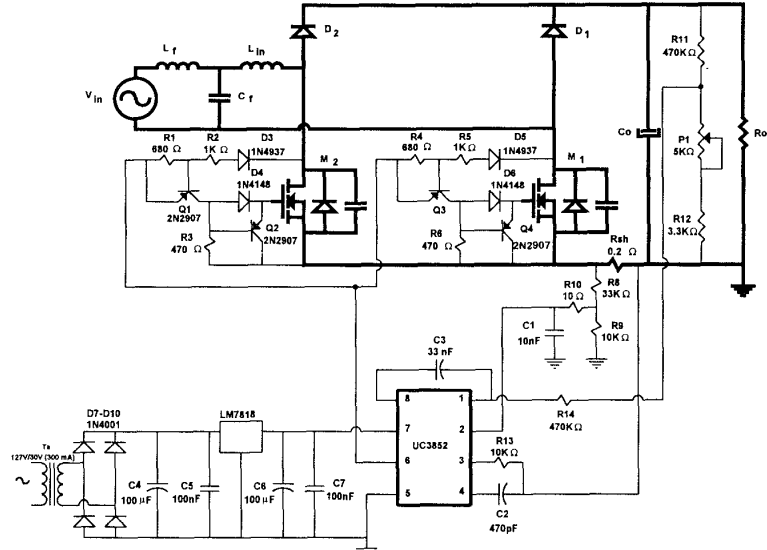


Fig. 11 - Complete Diagram of the Implemented Prototype.

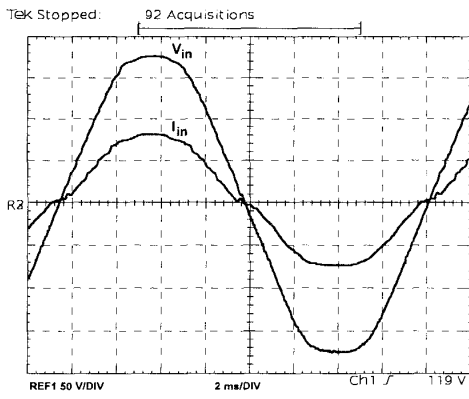


Fig. 12 - Input voltage (50 V/div.) and input current (2 A/div.).

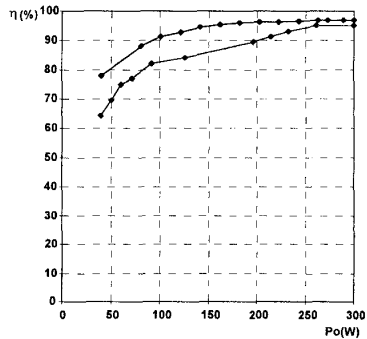


Fig. 13- Efficiency in the semi-resonant converter (up) and in the hard-switched converter (down).

The comparison between individual harmonic components of the input current and the IEC-555-2 standard is shown in Table I. It can be verified that the prototype complies with this standard.

The input inductor current is shown in Fig. 14. The input inductor peak current naturally follows the sinusoidal input voltage.

In Fig. 15 it is shown the voltage across the MOSFET M₁. It can be noticed that this voltage is clamped on the output voltage V_o. The commutation detail of the MOSFET M₁ is shown in Fig. 14. As can be verified, the ZVS commutation is achieved.

Table I - Experimentally obtained harmonic spectrum compared with IEC 555-2 standard.

Harmonic Order	Experimental Results (A rms)	IEC 555-2 Standard (A rms)
3rd	0.1050	1.956
5th	0.1350	1.087
7th	0.0161	0.815
9th	0.0238	0.543
11th	0.0153	0.326
13th	0.0035	0.276
15th	0.0061	0.239
17th	0.0062	0.211

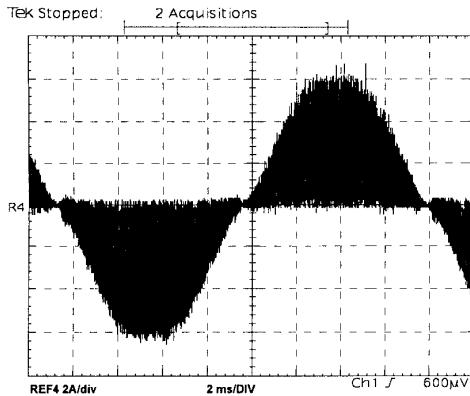


Fig. 14 - Input inductor current (2 A/div.).

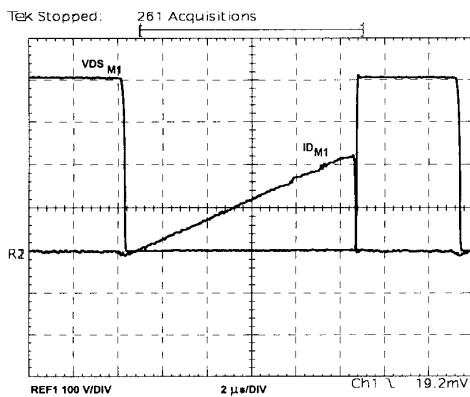


Fig. 15 - Drain-to-source voltage (100V/div.) and drain current (2A/div.) of MOSFET M1.

The voltage and current of diode D_1 are shown in Fig. 16. It is verified that the current through the diode naturally extinguishes, therefore, the effect of the diode reverse recovery will be negligible.

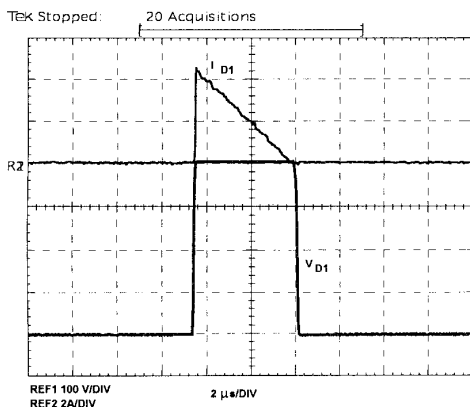


Fig. 16 - Voltage (100 V/div.) and current (2A/div.) of diode D_1 .

VII - CONCLUSION

In this paper a technique to improve the efficiency of power factor correction rectifiers, by reducing the commutation losses and the conduction losses is presented. The high efficiency is obtained by three important factors:

- the soft-switching (ZVS);
- there are only two semiconductor voltage drops in the current flow path at any time;
- the conduction losses in the MOSFET's are reduced if the gate-to-source voltage is high when the current is flowing from source to drain.

The topology also presents the following characteristics:

- The absence of auxiliary switches to perform the soft-commutation;
- Capability to draw a sinusoidal input current with constant on time of MOSFET M_1 and M_2 , using critical conduction mode with variable switching frequency.

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