

A Unity Power Factor Rectifier Based on a Two-Cell Boost Converter Using a New Parallel-Connection Technique

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*Abstract*¹ - This paper applies a recently introduced parallel-connection technique to a boost converter with power factor correction. By mean of a small extra inductance two MOSFET-PWM cells are associated in parallel, leading to an improved performance and reliable switched converter, along with simplified layout requirements. A comparison of the structure used in this paper with some alternative techniques is also provided.

A simplified mathematical analysis of the main circuit, based on the PWM-switch model, is also presented along with digital simulation results.

Results from a 3kW-70kHz prototype operating with power-factor correction (PFC) and soft commutation show that the technique is very useful. It is capable to reduce diode reverse-recovery problems, increasing the efficiency of the converter and also improving the overall reliability.

I. INTRODUCTION

Power factor correction strategies for switching power supplies have been object of many scientific works during the past few years [1], [2], [3], [4]. For a single-phase off-line switching regulator much effort has been made to reach the 3 kW mark with reliability, efficiency and compactness [5], [6]. The optimization process for a single PWM-cell converter depends on matching the MOSFET switching behavior to the dynamic characteristics of the companion fast recovery diode, and to the physical layout of the power stage to minimize over voltage transients and excessive EMI. Using a two-cell interleaved converter [7] one can get a great power density without the penalty of reduced power-conversion efficiency (due to higher frequencies with no increase of switching losses). However, interleaving requires a complex circuitry leading to a more expensive implementation and reduced reliability. Moreover, the unequal current sharing in continuous-inductor current and at average current control is a practical problem in this case [6]. The interleaving strategy is a kind of cellular architecture, for which a number of autonomous converters share the total power allowing the employ-

ment of single-die inexpensive devices [8], [9]. Of course one can expect that the losses due to semiconductor conduction are going to be reduced to the half of the single switch counterpart. So, the double-switch option increases the efficiency and saves heatsink area (reducing the weight and volume) for the final converter.

This paper proposes the application of a recently introduced parallel-connection technique to a boost PFC converter, which offers a good alternative to the strategies mentioned above. The main advantages include a good static and dynamic current balance along with a simplified requirement for the power stage layout, since under certain limits stray inductances do not interfere in the current distribution process [10]. Moreover, the diode reverse recovery process is divided by two devices. As will be shown, the current procedure allows to reduce current sensor losses due to a particular feature of the new technique.

Fig.1 shows the generic parallel-connection cell and Fig.2 shows its application to a boost converter, which consists on the proposed power stage for this work.

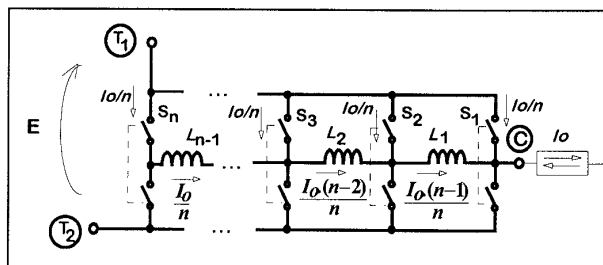


Figure 1- Generalized cell for the new paralleling technique

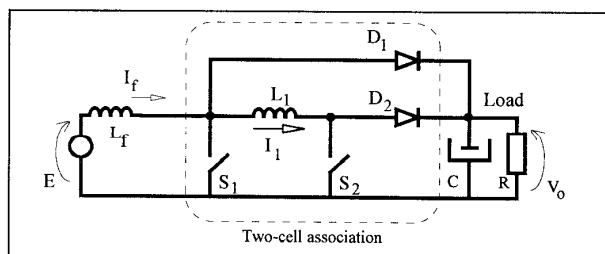


Figure 2- Two-cell boost converter

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In Fig.2 the PWM cell (any two switches connected by dashed lines in Fig.1) has been adapted to work with an active switch on the upper side and a diode on the lower side. Fig.3 shows the overall system, including a block diagram of the control circuit.

From Fig.3 one can notice that both switches are gated by the same gate signal, which determines a great simplicity and reliability to the proposed converter. Another benefit of the new technique consists in that a switch does not support all the input current i_f , for any reason, it remains conducting alone[9]. This is a potential problem in the conventional paralleling technique [11].

As will be proved later, the shunt resistor may be transferred to the balance inductor branch, in order to reduce the converter losses. That possibility enlarges the advantages of the proposed technique.

The current reference block of Fig.3 is based on the rectifier voltage output, which is a "positive" sinusoidal variable. The employed control strategy imposes a continuous conduction current through the boost inductor, L_f . So, the converter operates in the continuous conduction mode, or CCM.

Fig.4 shows the ideal waveforms assuming negligible ripple over inductor currents and output voltage.

II. BASIC TWO-CELL BOOST THEORETICAL ANALYSIS

Fig.5 shows a simplified equivalent circuit for Fig.2 using the line-to-output PWM-switch model [12]. In that figure all the switches have been represented by a "time-average" resistance, r , which is based on the ON-resistances of the active and passive switches. For the purpose of this analysis some parameters have been neglected such as the parasitic resistances of the reactive elements.

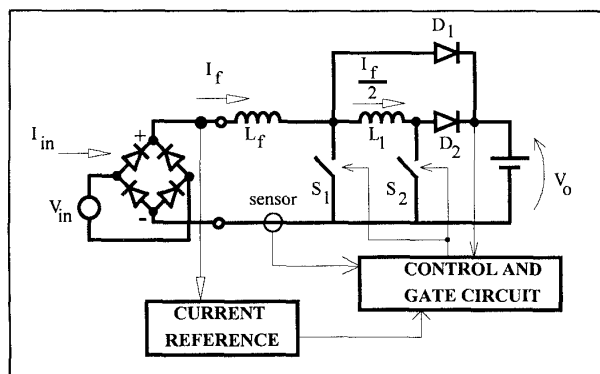


Figure 3- Two-cell, PFC boost converter

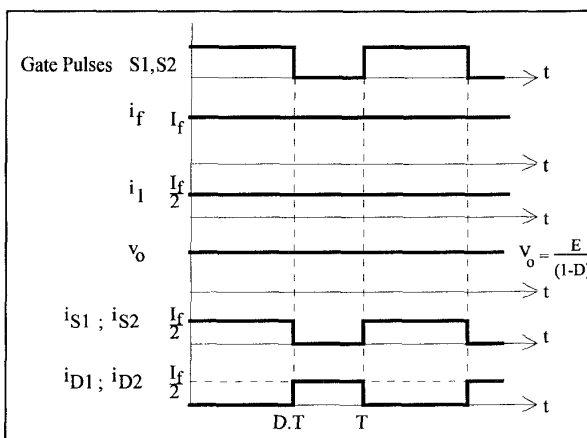


Figure 4- Boost ideal waveforms

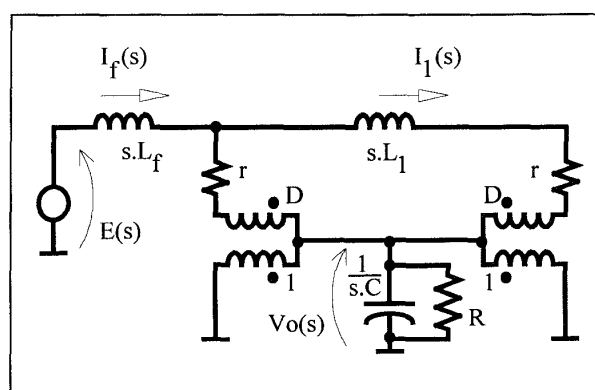


Figure 5- Line-to-output model

The importance of the model in Fig.5 grounds on the fact that no closed loop strategy is going to be used to control the current sharing among switches. So, these currents must reach the dynamic and static current equilibrium by a natural operation way. From Fig.5 it is possible to find the transfer-functions of the main variables, such as v_o , i_f and i_1 :

$$\begin{aligned} \frac{V_o(s)}{E(s)} &= \frac{(1-D)(2.r + L_1.s).R}{H(s)}; \\ \frac{I_f(s)}{E(s)} &= \frac{(1+R.C.s)(2.r + L_1.s).R}{H(s)}; \\ \text{and } \frac{I_1(s)}{E(s)} &= \frac{(1+R.C.s).r}{H(s)}. \end{aligned} \quad (1)$$

Where $H(s)$ can be reduced to:

$$H(s) = L_f \cdot L_1 \cdot C \cdot R \cdot s^3 + L_f \cdot (L_1 + 2 \cdot r \cdot R \cdot C) \cdot s^2 + [r^2 \cdot R \cdot C + L_1 \cdot R \cdot (1 - D)^2 + 2 \cdot L_f \cdot r] \cdot s + 2 \cdot R \cdot r \cdot (1 - D)^2 \quad (2)$$

if one consider a practical situation, in which $r \ll R$ and $L_1 \ll L_f$

Fig.6 and Fig.7 show the performance of the basic boost converter using $E=50V$, $f=50$ kHz, $D=0.5$, $L_f=1mH$, $L_1=14\mu H$, $C=100\mu F$ and $R=10\Omega$. The gate pulses to switch S_2 has been delayed 60ns, to show the current damping capability of the structure. The model equation (1) has been included in Fig.6 revealing a very good description of the simulation case, in such a way that their curves are almost the same of their simulated counterparts.

III. PFC TWO-CELL BOOST MODELING

The previous section analysis has shown that the two-cell basic boost converter has a good static and dynamic characteristic, revealing a current damping capability. Another important point to be checked is related to the control-to-output behavior of the final PFC converter. To study this subject the circuit of Fig.3 is going to be modeled by a procedure similar to that in previous section, as shown in Fig.8. In that circuit the output branch has been simplified to a constant output voltage source, V_o , being in rest in the equivalent model.

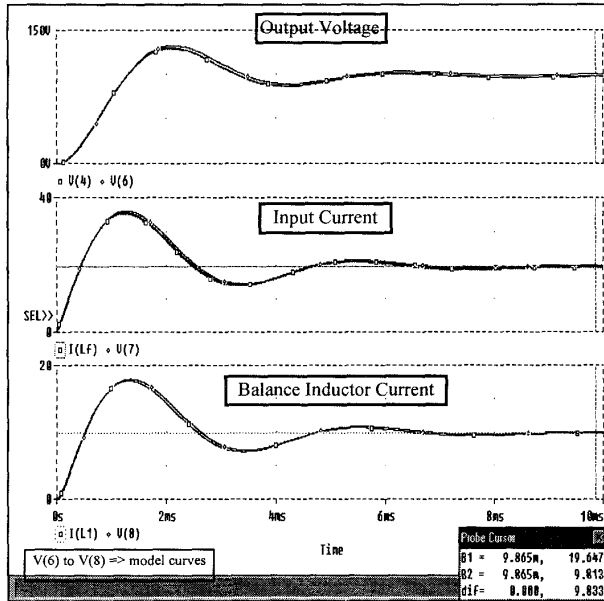


Figure 6- Voltage-step response (simulation and model)

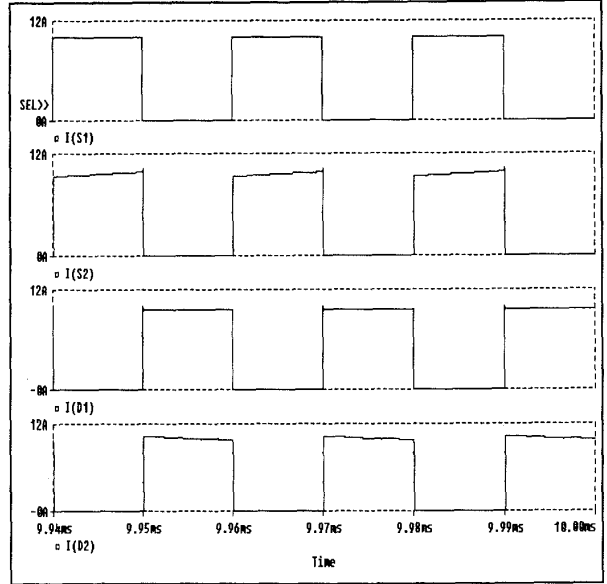


Figure 7- Static current sharing

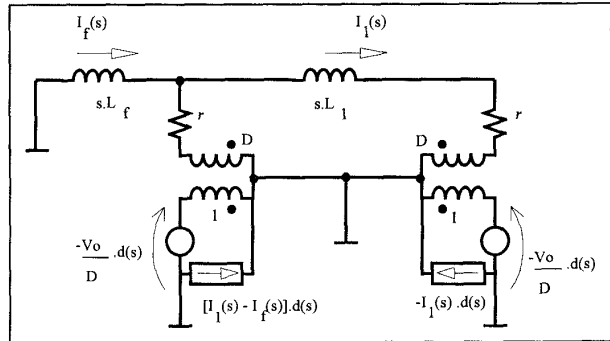


Figure 8- Control-to-output model of the PFC boost converter

Equations (3)a and (3)b show the transfer functions of inductor currents, obtained by solving the circuit of Fig.8.

$$\begin{aligned} \frac{I_f(s)}{d(s)} &= \frac{V_o \cdot (2 \cdot r + s \cdot L_1)}{L_f \cdot L_1 \cdot s^2 + (L_f \cdot 2 \cdot r + r \cdot L_1) \cdot s + r^2} \\ \frac{I_1(s)}{d(s)} &= \frac{V_o \cdot r}{L_f \cdot L_1 \cdot s^2 + (L_f \cdot 2 \cdot r + r \cdot L_1) \cdot s + r^2} \end{aligned} \quad (3)$$

It is not difficult to show that, for practical situations (changes in d around 120 Hz and $L_1 \ll L_f$) equations (3)a and (3)b reduce, at a certain frequency range spread over the 120 Hz mark, to:

$$\frac{I_f}{d(s)} = \frac{V_o}{s.L_f} \text{ and } \frac{I_1}{d(s)} = \frac{V_o}{s.2.L_f}. \quad (4)$$

So, the current through balance inductor L_1 is the half of the input current, from the control viewpoint. This means that the position of the current sensor can be transferred to the balance inductor branch, which may be used to reduce the losses in the final converter. Statement (4)b can be verified by the Bode plot of Fig.9, using $V_o=50V$, $L_o=1mH$; $L_1=14 \mu H$; $r=0.1 \Omega$ in equation (3)b.

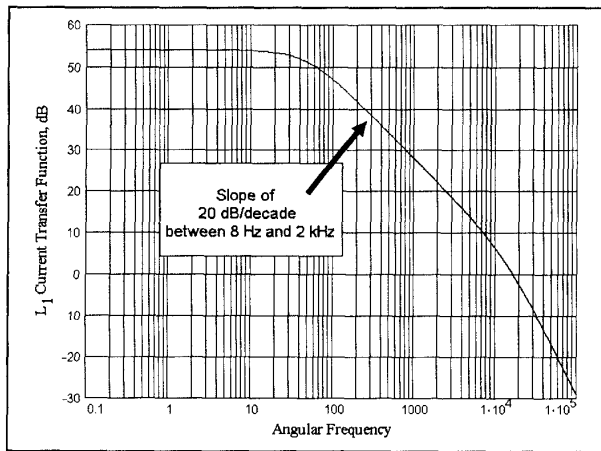


Figure 9- Bode plot for equation (3)b.

In order to verify those basic assumptions the circuit of Fig.3 has been simulated using a PI current control strategy (average current control). The simulation parameters are: $V_{in}=220V_{rms}$; $f=60$ Hz; $L_f=700 \mu H$; $L_1=10 \mu H$, $V_o=400V$, $P_o=3.2$ kW, $f_{sw}=70$ kHz. It has been employed a soft-commutation technique, which will be clear in the next section. It has been chosen Pspice models for the IRFP460, as active devices, and MUR850 for diodes.

Fig.9 and Fig.10 show the simulation results using the above mentioned set of parameters. The current sense resistor has been inserted in the same branch as the balance inductor element.

Fig. 9 shows that a high power factor situation has been attained. Fig. 10 reveals that an excellent current distribution among switches has been reached.

IV. EXPERIMENTAL RESULTS

The parallel-connection technique explained in this paper has been tested in a boost-based pre-regulator switched power supply, employing power factor correction control and a soft commutation technique, as shown in Fig. 12.

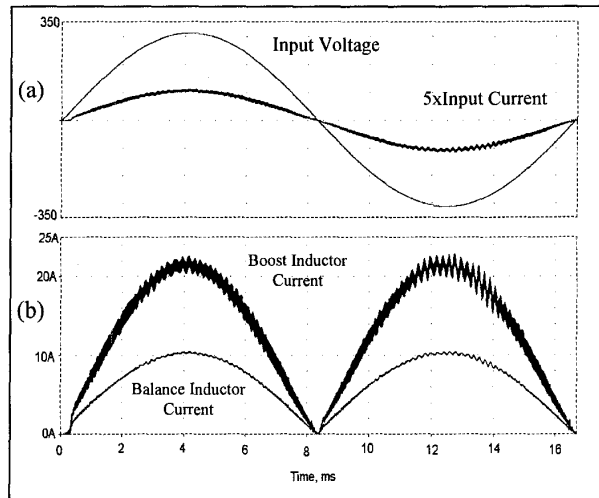


Figure 10- Waveforms from computer simulation
a) Utility voltage and current
b) Boost and balance inductor currents

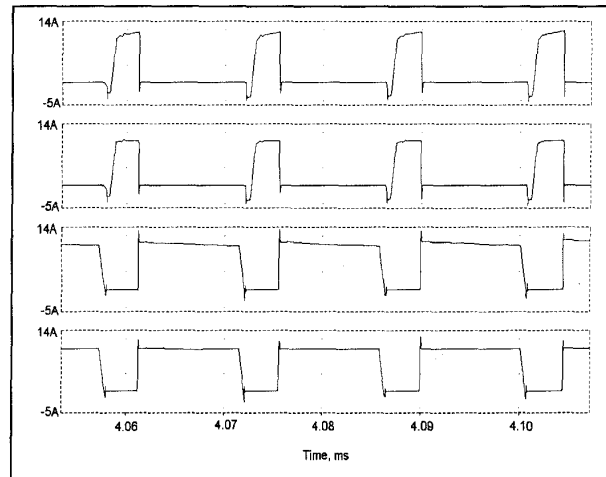


Figure 11- Device Currents Comparison
(From top to bottom: S_1 , S_2 , D_1 , D_2 currents at peak condition)

Fig. 12 shows a simplified diagram of the laboratory prototype. The basic power circuit is constituted of a couple of PWM cells (two sets of a PWM switch formed by a diode and a MOSFET) connected by mean of a $10 \mu H$ inductor. This stage is fed by a full-bridge rectifier output, boosted by a $700 \mu H$ inductor. On the other side a zero-voltage transition (ZVT) [13] arrangement is set to provide the soft-commutation feature. This auxiliary circuit employs more three diodes, another MOSFET and a $10 \mu H$ inductor. Those components are expected to work with only a small fraction of the total proc-

essed energy. All the active devices are gated and controlled by a control unity based on the 3854 Unitorde's integrated circuit [14]. This stage is designed to gate the MOSFET's at a 70 kHz frequency.

Despite the alternative to put the current sensor in the balance inductor branch, as discussed in last section, the laboratory structure used the conventional position (sensing the input current). A future set-up is being planned to verify and adapt the structure to the new way of current sensing.

The measured output power reached a value of 3.04 kW, leading to an efficiency of 97.5%. This mark could be enlarged if the alternative sensing way had been adopted.

Fig. 13 shows the complete circuit diagram useful to anyone who wants to reproduce the results that follow.

Fig. 14 shows the voltage and current measured at the input of the thyristor semi-controlled full-bridge rectifier. The current is completely in phase with the voltage and follows its shape, which has already a little distortion from an ideal sinusoidal waveform. Naturally, this result ensures a very high power factor value, near unity.

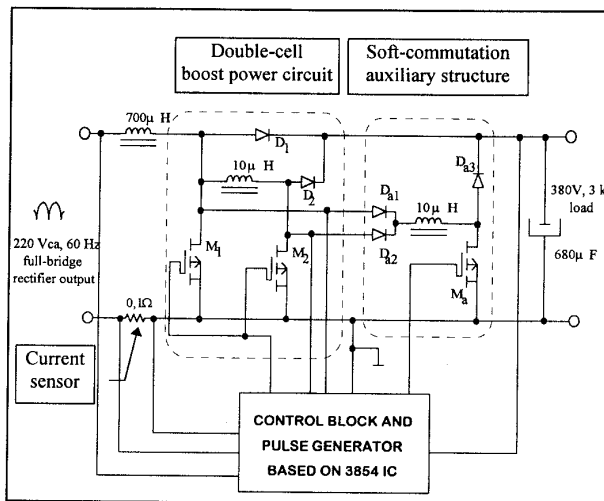


Figure 12- Pre-Regulator Circuit Tested in Laboratory (Simplified Diagram)

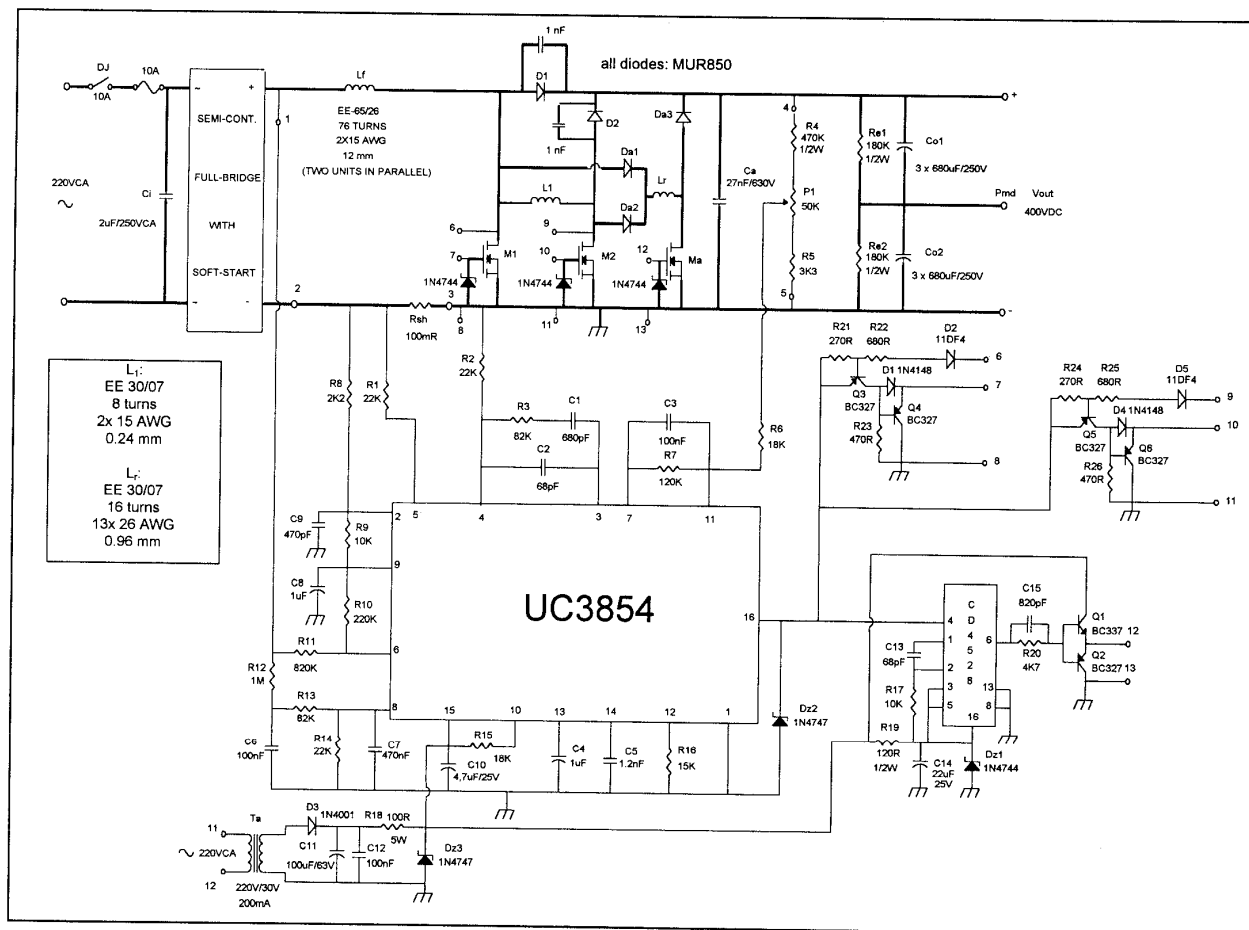


Figure 13: Complete Circuitry of Laboratory Prototype

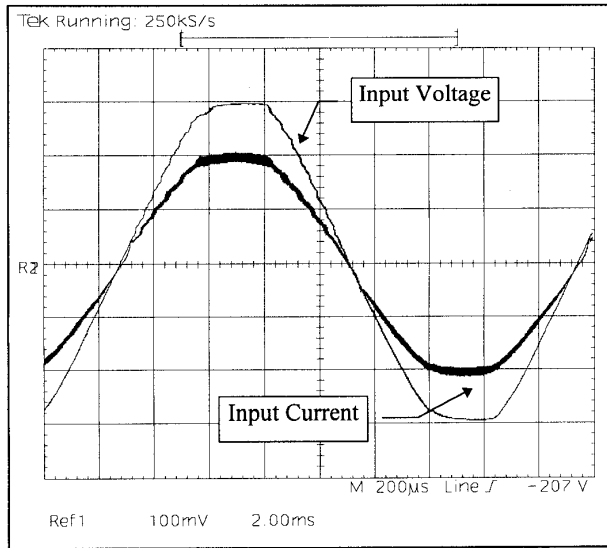


Figure 14. Input Voltage and Current at full load (100 V/div; 10A/div)

Fig. 15 shows the waveforms of the boost and the balance inductor currents. As predicted, the balance inductor current is the half of the value measured for the boost inductor current. This is a fundamental condition for a good current balance among the main semiconductor devices. This situation is definitely proved in Fig. 16. At the peak condition one can observe a very good current distribution. Fig.16 also shows that the diode reverse recovery problem [5] is minimized, since it has been shared between two diodes. So, it is expected a reduced overvoltage over diodes and as a consequence lower EMI levels.

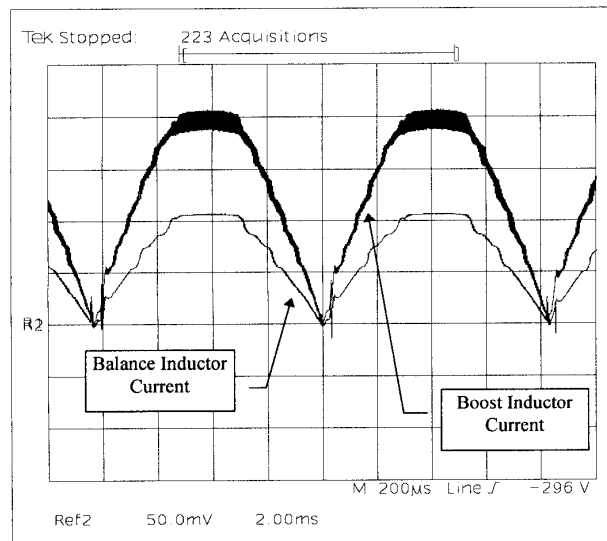


Figure 15- Input and Balance Inductor Currents (5 A/div)

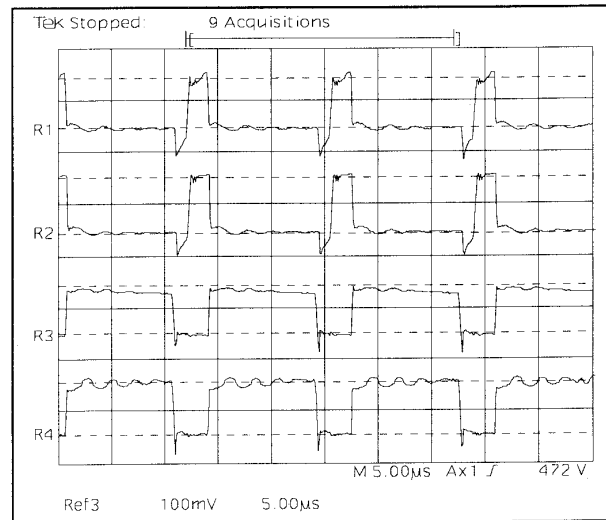


Figure 16- Device Current Comparison at Peak Condition (from top to bottom: M₁, M₂, D₁ and D₂; 5A/div)

Fig. 17 shows a detail of the soft-commutation process. It can be noticed that the device drain current flows by its anti-parallel diode only after the drain voltage falls to zero. So, the positive current conduction is assured to start at zero voltage condition. At turn-off, the MOSFET drain-to-source capacitance needs to be charged, which explains the energy exchange observed during this transition.

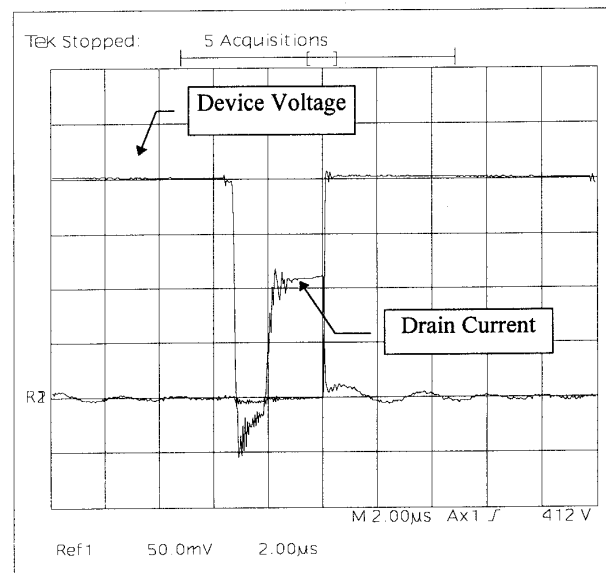


Figure 17. Soft Commutation Detail. (100V/div, 5A/div)

V. CONCLUSIONS

This work has shown an application of a recently introduced parallel-connection technique to a rectifier system with unity power factor. That system is based on a two-cell boost converter, from which one can expect:

- a good power distribution obeying the cellular concept;
- an excellent static and dynamic distribution of currents;
- simplified a layout requirements (due to a natural feature of the structure and the diode reverse recovery shared by two devices);
- reliability due to its simplicity
- high efficiency;
- unity power factor
- and a reduction of sensor losses.

A laboratory prototype, which proved the above features, has been implemented using a soft-commutation technique and the following parameters: 3.04 kW output power, 380V dc voltage, 70 kHz switching frequency, with an overall efficiency of 97.5%.

VI. REFERENCES

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