

Zeta Converter With High Power Factor Operating in Continuous Conduction Mode

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Abstract: This paper presents the analysis of the ZETA converter operating in continuous conduction mode (CCM) for power factor correction. The main attractive of the ZETA converter is that it is a naturally isolated structure, which allow a regulated output voltage with only one power processing stage. Principle of operation, mathematical analysis and experimental results are presented.

1. INTRODUCTION

Several topologies have been researched in search of a structure which not only is able to fulfill the requirements of the power factor and the amount of harmonics injected in line foreseen in the norms, but which would also show the best ensemble of characteristics.

Although being the most frequently employed and studied structure, the Boost converter presents some limitations in its application, for it is not naturally isolated structure and because it only operates as step up voltage. As alternative to these limitations it was proposed and developed the study of the Zeta converter operating in discontinuous mode applied to the power factor correction [3]. The Zeta converter showed itself as very attractive because it operates as step up as well as step down voltage, beside the fact of being a naturally isolated structure and processing power at one single stage.

But in applications which imply high power, the operation of a converter in discontinuous mode is not attractive because it results in high rms values of the currents causing high levels of stress in the semiconductors. Aiming to extend the alternative by using of the Zeta converter in power factor correction to applications in higher powers, and having in mind the main characteristics end advantage of this converter in face of the limitations of the Boost converter, this paper presents the study of the Zeta converter operating in continuous conduction mode for power factor correction by using the average current mode control.

2. PRINCIPLE OF OPERATION

The Fig. 1 presents the Zeta converter for power factor correction with the input filter (C_f , L_f).

To simplify the analysis and the comprehension, the following assumptions are made:

- The circuit operation is steady state.
- The semiconductors are considered ideals.

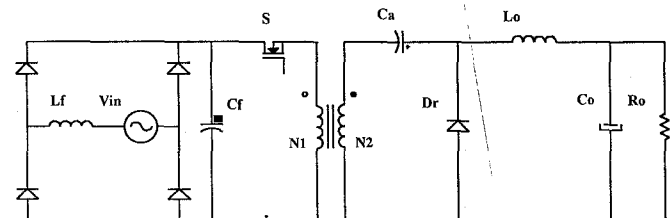


Fig. 1 - ZETA converter AC/DC

- The transformer is considered by its magnetizing inductance and referred to the primary side.
- The capacitor C_o is large enough to make its voltage constant and equal to V_o .
- The line voltage is constant in a switching period.

By referring the secondary side parameters to the primary side, the circuit shown in Figs. 2 and 3 will be obtained, where :

$$V_o' = a \cdot V_o ; C_a' = C_a / a^2 ; C_o' = C_o / a^2 ; L_o' = a^2 \cdot L_o ; R_o' = a^2 \cdot R_o ; a = N1 / N2 \text{ and } V_{in} = V_{pk} \cdot \sin(\omega t) \quad (1)$$

2.1. Operation Stages

The converter Zeta operating in continuous conduction mode has two operation stages:

1st Stage (0,DT) - Fig. 2 : Switch S is conducting, the line source supply energy to the L_m' inductance and the capacitor C_a' supply energy to L_o' , current $i_{L_m'}$ and $i_{L_o'}$ increase linearly. Voltages $V_{C_o'}$ and $V_{C_a'}$ are considered constants and equals to \dot{V}_o' .

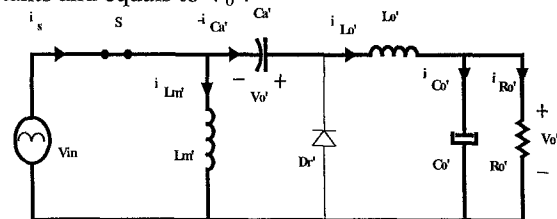


Fig. 2 - First stage

2nd Stage (DT,T) - Fig. 3 : By the time "DT", S is turned off and the diode D_r' starts to conduct allowing that L_m' and L_o' transfer their energy to C_a' and C_o' respectively. At second stage do not have energy circulation in the line, which assure us that do not have harmonic distortion in the current line.

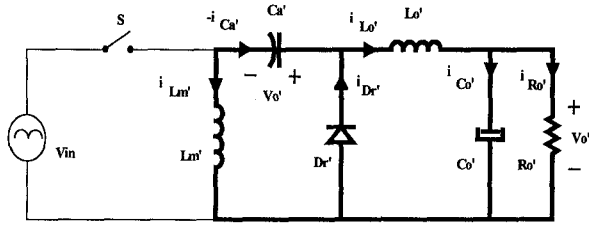


Fig. 3 - Second stage

The Fig. 4 show the main waveforms in one switching period (t_0 to t_2):

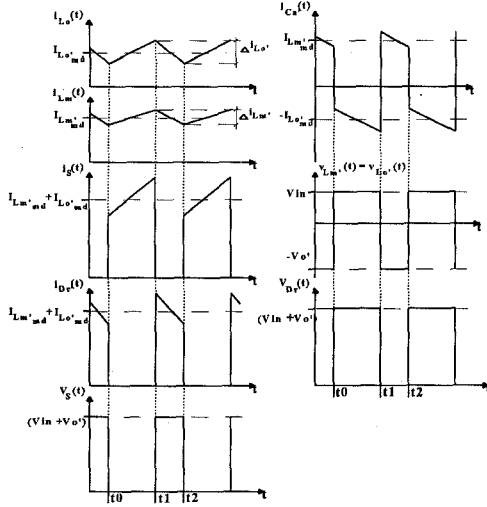


Fig. 4 - Main waveforms

2.2. Mathematical Analysis

2.2.1. Switching period

In order to facilitate the understanding of the values of current and voltage defined in a switching period will be referred as instantaneous values. In a switching period the line voltage can be considered constant and therefore the operation of the converter in this period can be analyzed as the operation of Zeta DC/DC converter [1,2]. As it refers to a previously developed study, only main relations will be stated:

A) Output characteristics

$$\frac{V_0'}{V_{in}} = \frac{D}{(1-D)} \quad (2)$$

$$\frac{I_{in_md}}{I_{Lo'_md}} = \frac{D}{(1-D)} \quad (3)$$

B) Instantaneous average current through L_m' and D_r'

$$I_{Lm'_md} = I_{in_md} \quad (4)$$

$$I_{Dr'_md} = I_{Lo'_md} \quad (5)$$

C) Current ripple through the inductors

$$\Delta i_{Lm'} = \frac{V_{in}}{L_m'} \cdot D \cdot T_s \quad (6)$$

$$\Delta i_{Lo'} = \frac{V_{in}}{L_o'} \cdot D \cdot T_s \quad (7)$$

D) Voltage Ripple on capacitor C_a'

$$\Delta V_{Ca'} = \frac{I_{Lm'_md} \cdot (1-D) \cdot T_s}{C_a'} \quad (8)$$

2.2.2. Line Period

In order to displaced the harmonics of the input current (current through the switch) to high frequencies the average current mode control acts in the input current making its instantaneous average value vary the same way and with the same instantaneous average value of the desired fundamental current. Thus, during half period of line we have:

$$V_{in} = V_{pk} \cdot \sin(\omega t) \quad (9)$$

$$I_{in_md} = I_{pk} \cdot \sin(\omega t) \quad (10)$$

$$I_{pk} = \frac{2 \cdot P_{in}}{V_{pk}} \quad (11)$$

A) Duty-cycle

By replacing Eq. (9) in Eq. (2) we obtain:

$$D = \frac{1}{[1 + \alpha \cdot \sin(\omega t)]} \quad (12)$$

$$\text{Where: } \alpha = \frac{\Delta V_{pk}}{V_0'}$$

Fig. 5 shows the variation of duty-cycle during half period of line to different values of α .

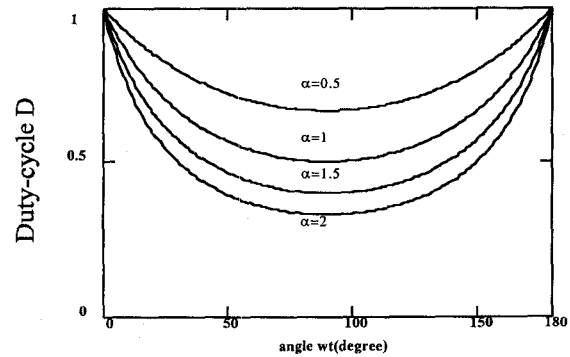


Fig. 5 - Duty-cycle

B) Instantaneous average current through the inductors

By replacing Eqs. (10) and (12) in Eqs. (3) and (4) the variation of the instantaneous average current through the inductors during half period of line is obtained:

$$I_{Lo'_md} = \alpha \cdot I_{pk} \cdot \sin^2(\omega t) \quad (13)$$

$$I_{Lm'_md} = I_{pk} \cdot \sin(\omega t) \quad (14)$$

In case there are not losses, the input power is equal to the output power and this way from Eq. (11) it is obtained:

$$I_{pk} = \frac{2 \cdot V_0 \cdot i_0'}{V_{pk}} = \frac{2 \cdot i_0'}{\alpha} \quad (15)$$

By replacing Eq. (15) in Eq. (13) and referring to the secondary, the variation of the instantaneous average current through the inductor L_0 of the output filter is obtained:

$$I_{L_{0md}} = 2 \cdot i_0' \cdot \sin^2(\omega t) \quad (16)$$

C) Current ripple through the inductors

By replacing Eqs. (9) and Eq. (12) in Eq. (6) and some manipulations it leads to the normalized current ripple through inductor L_m' :

$$\frac{\Delta i_{L_m'}}{V_{pk}} = \frac{\Delta i_{L_m'} \cdot L_m' \cdot f_s}{V_{pk}} = \frac{\sin(\omega t)}{[1 + \alpha \cdot \sin(\omega t)]} \quad (17)$$

By replacing Eqs. (9) and Eq. (12) in Eq. (7) and some manipulations it leads to the normalized current ripple through the inductor L_0' already referred to the secondary.

$$\frac{\Delta i_{L_0}}{V_0} = \frac{\Delta i_{L_0} \cdot L_0 \cdot f_s}{V_0} = \frac{\alpha \cdot \sin(\omega t)}{[1 + \alpha \cdot \sin(\omega t)]} \quad (18)$$

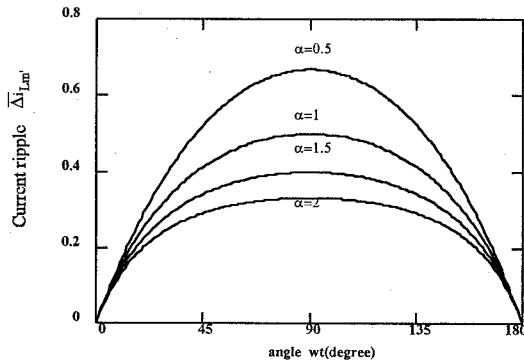


Fig. 6 - Normalized current ripple through L_m' during half period of line

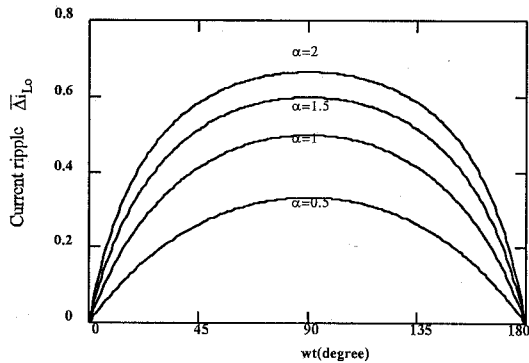


Fig. 7 - Normalized ripple of current through L_0 during half period of line

D) Voltage ripple on capacitors

By replacing Eqs. (12), (14) and (15) in Eq. (8) and with some manipulations it leads to the normalized voltage ripple on capacitor C_a' already referred to the secondary:

$$\frac{\Delta V_{C_a}}{V_0} = \frac{f_s \cdot \Delta V_{C_a} \cdot C_a}{2 \cdot i_0} = \frac{\sin^2(\omega t)}{[1 + \alpha \cdot \sin(\omega t)]} \quad (19)$$

From alternate components of the current through the output inductor L_0 which move through the output capacitor

C_0 we can consider the second order component having in mind that the other components have much lower amplitudes and much higher frequencies. Thus it is obtained from Eq. (16):

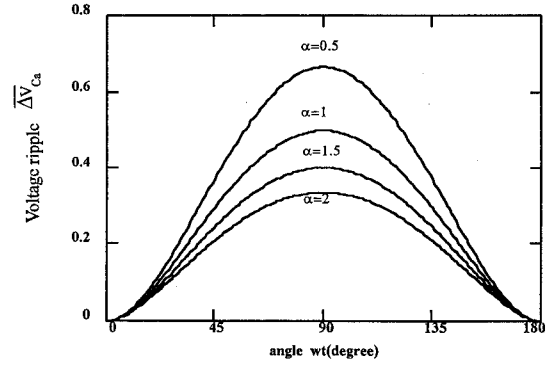


Fig. 8 - Normalized voltage ripple on C_a during half period of line

$$i_{C_0}(t) = -i_0' \cdot \cos(2 \cdot \omega t) \quad (20)$$

$$v_{C_0}(t) = \frac{1}{C_0} \int i_{C_0}(t) dt \quad (21)$$

By manipulating Eqs. (20) and (21) the amplitude voltage ripple of second order (120Hz) on the output capacitor C_0 is obtained:

$$V_{C_{0r}} = \frac{P_0}{2 \cdot \pi \cdot 120 \cdot V_0 \cdot C_0} \quad (22)$$

E) Peak voltage through semiconductors.

In observing Fig. 4 it is noted that the voltage in the semiconductors corresponds to the amount of the line voltage and output voltage. Thus, the maximum voltage in semiconductors occurs when the input voltage is the greatest, that is, when $(\omega t) = 90^\circ$. By referring the voltage on the diode to the secondary we obtained:

$$V_{S_{pk}} = V_{pk} + V_0' \quad (23)$$

$$V_{D_{rpk}} = \frac{V_{pk}}{a} + V_0 \quad (24)$$

By normalizing Eqs. (23) and (24) the normalized peak voltage trough the semiconductors is obtained:

$$\frac{V_{S_{pk}}}{V_{pk}} = \frac{(1 + \alpha)}{\alpha} \quad (25)$$

$$\frac{V_{D_{rpk}}}{V_0} = (1 + \alpha) \quad (26)$$

F) Average current through the diode

According to Eq. (5) the instantaneous average current trough the diode is equal to the instantaneous average current through the inductor (L_0) of the output filter. Therefore from Eq. (16) the average current through the diode in half period of line, already referred to the secondary is defined:

$$i_{D_{rmt}} = i_0 \quad (27)$$

G) RMS current through the switch

By accomplishing an approximate calculation of the rms current through the switch, the current ripple trough the

inductors will be rejected, considering that under continuous conduction mode the current ripple is much smaller than the instantaneous average value. Thus from Eqs. (13) and (14) it is obtained:

$$i_{Lm'}(t) = I_{pk} \cdot \sin(\omega t) \quad (28)$$

$$i_{Lo'}(t) = \alpha \cdot I_{pk} \cdot \sin^2(\omega t) \quad (29)$$

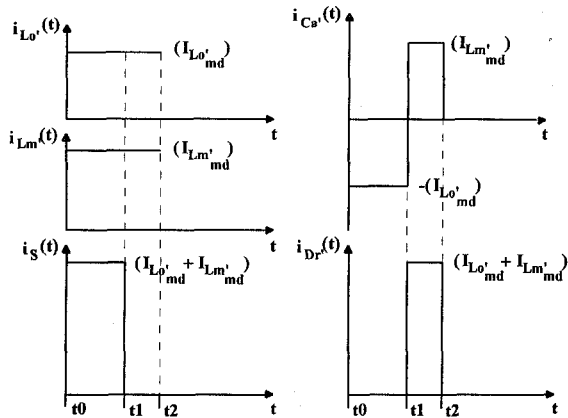


Fig. 9 - Approximate current

By observing Fig. 9 the current through the switch is defined:

$$i_S(t) = i_{Lm'}(t) + i_{Lo'}(t) \quad 0 < t < D \cdot T_s \quad (30)$$

By replacing Eqs. (28) and (29) in Eq. (30) and integrating the rms current through the switch in a switching period is defined:

$$I_{S_{ef}}^2 = I_{pk}^2 \cdot \sin^2(\omega t) [1 + \alpha \cdot \sin(\omega t)] \quad (31)$$

By integrating during half period of line and by normalizing the Eq. (31) the normalized rms current through the switch is obtained:

$$\bar{i}_{S_{ef}} = \frac{I_{S_{ef}}}{I_{pk}} = \sqrt{\frac{1}{\pi} \int_0^\pi \sin^2(\omega t) \cdot [1 + \alpha \cdot \sin(\omega t)] d(\omega t)} \quad (32)$$

$$\bar{i}_{S_{ef}} = \frac{I_{S_{ef}}}{I_{pk}} = \sqrt{\left(\frac{4}{3 \cdot \pi} \cdot \alpha + \frac{1}{2}\right)} \quad (33)$$

Fig. 10 shows the variation of the rms current through the switch in function of parameter α .

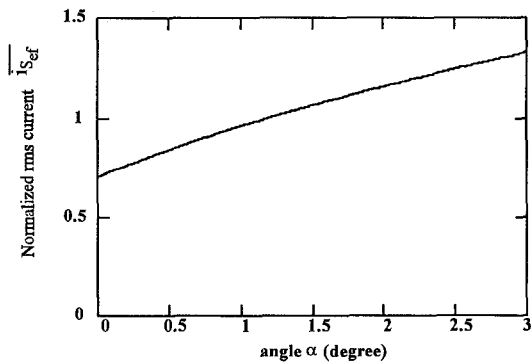


Fig. 10 - Normalized rms current through the switch

H) Peak current through the semiconductors

According to the Eqs. (13), (14), (17) and (18) the maximum instantaneous average current value and the maximum current ripple through the inductors occur to $(\omega t)=90^\circ$ and, thus, according to Eq. (30) the peak current through the semiconductors also occur to $(\omega t)=90^\circ$.

By observing Fig. 4 the peak current to $(\omega t)=90^\circ$ is defined:

$$i_{S_{pk}} = i_{Dr'_{pk}} = i_{Lm'_{pk}} + i_{Lo'_{pk}} \quad (34)$$

Where:

$$i_{Lm'_{pk}} = \left[I_{Lm'_{md}}(90^\circ) + \frac{\Delta i_{Lm'}(90^\circ)}{2} \right] \quad (35)$$

$$i_{Lo'_{pk}} = \left[I_{Lo'_{md}}(90^\circ) + \frac{\Delta i_{Lo'}(90^\circ)}{2} \right] \quad (36)$$

2.3 Control Method

The average current mode control is characterized by the presence of a pole in the origin of the response in frequency of the loop compensation of the current [6]. The main attractives in the employment of this controlling method are [5,6]:

- high degree of accuracy in the reproduction of reference;
- It monitors and controls the current in any part of circuit including the current in the switch and the diode;
- Indifferent concerning the operation mode of the converter, CCM or DCM.

The implementation of the average current mode control through a dedicate integrated circuit [6,7] becomes simple allowing the total control of the structure due to the functions that this integrated circuit incorporates. Besides the loop of compensation of current and of the generation of the reference current, the integrated circuit incorporates:

- External loop of compensation of output voltage responsible for the control of the flux power;
- Feedforward of the line voltage suits the line current to the variations of the line voltage;
- Limitation of the peak current;
- Soft-start.

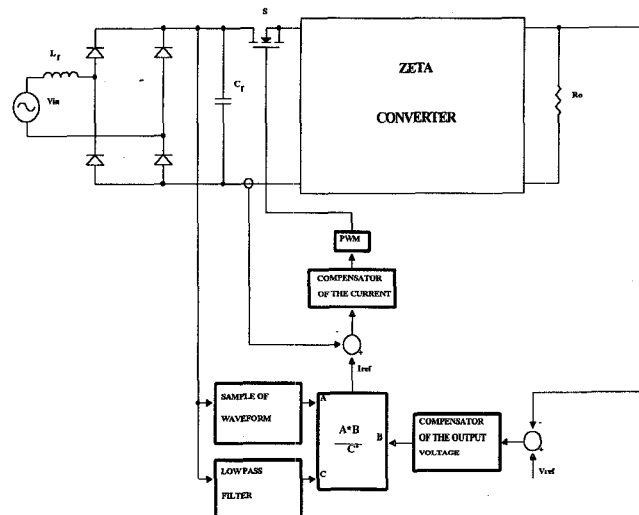


Fig. 11 - Block diagram of the power and control circuits

In order to control the current it was the compensator of one zero and two poles employed in the control of the Boost converter [6].

3. DESIGN PROCEDURE AND EXAMPLE

Next, the design procedure is presented assuming the prototype project as example. The project of a preregulator was chosen under the following specifications:

$$P_{in} = 250 \text{ W} \quad V_{in} = 311(\pm 10\%) \cdot \sin(\omega t) \text{ V}$$

$$V_0 = 400 \text{ V}$$

$$I_{in} = 1.6(+10\%) \cdot \sin(\omega t) \text{ A} \quad f_s = 40 \text{ kHz}$$

$$a = \frac{N_1}{N_2} = 1$$

By admitting 20% of maximum ripple current in the nominal conditions of operation, the values of the inductances are determined through Eqs. (17) and (18):

$$L_m' \geq \frac{V_{pk_{nom}}}{f_s \cdot \Delta i_{Lm'}(\alpha_{nom}, 90^\circ) \cdot (1 + \alpha_{nom})}$$

$$L_m' \geq \frac{311}{40000 \cdot 0.2 \cdot 1.6 \cdot (1 + 0.777)} = 13.6 \text{ mH}$$

$$L_0 \geq \frac{V_0}{f_s \cdot \Delta i_{L0}(\alpha_{nom}, 90^\circ) \cdot (1 + \alpha_{nom})}$$

$$L_0 \geq \frac{400}{40000 \cdot 0.2 \cdot 1.25 \cdot (1 + 0.777)} = 17.5 \text{ mH}$$

According to Eq. (19), the maximum parametrized ripple voltage on the capacitor C_a occurs to the minimum line voltage. By admitting 10% of maximum ripple voltage on the capacitor C_a through Eq. (19), it is obtained:

$$C_a \geq \frac{2 \cdot i_0}{f_s \cdot \Delta V_{Ca}(\alpha_{min}, 90^\circ) \cdot (1 + \alpha_{min})}$$

$$C_a \geq \frac{2 \cdot \left(\frac{250}{400}\right)}{40000 \cdot 0.1 \cdot 400 \cdot (1 + 0.7)} = 441 \text{ nF}$$

By admitting 1.5% of maximum ripple voltage on the capacitor C_0 of the output filter, from Eq. (22) it is obtained:

$$C_0 \geq \frac{P_0}{2 \cdot \pi \cdot 120 \cdot V_0 \cdot V_{Co_r}}$$

$$C_0 \geq \frac{250}{2 \cdot \pi \cdot 120 \cdot 400 \cdot \left(\frac{0.015 \cdot 400}{2}\right)} = 276 \mu\text{F}$$

According to the reference [3] it is determined the input filter (L_f, C_f):

$$C_f = 137 \text{ nF}$$

$$L_f = 20 \text{ mH}$$

4. EXPERIMENTALS RESULTS

With the values obtained it was implemented a prototype whose main results in nominal power are presented as follows:

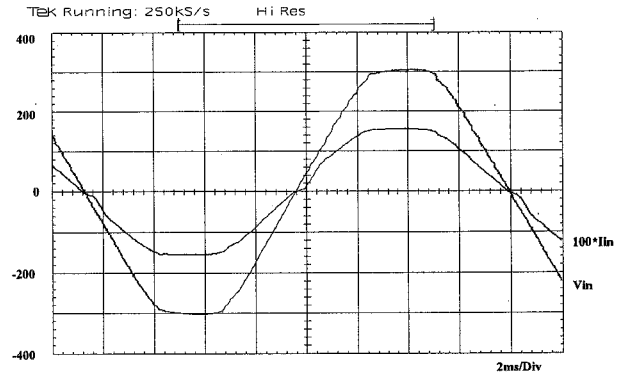


Fig. 12 - Line voltage (V) and current (A)

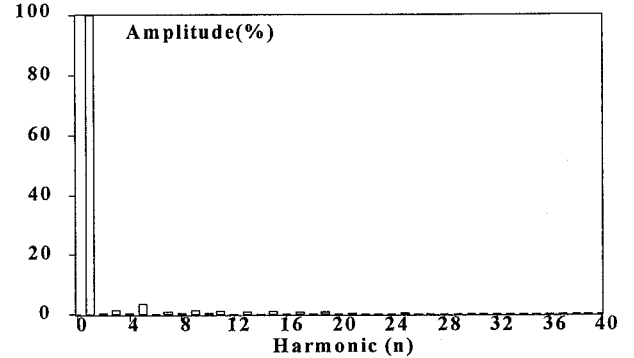


Fig. 13 - Current harmonic analysis

Fig. 12 presents the current and voltage of line where it can be noted the great proximity between the waveforms. Fig. 13 presents the harmonic analysis of the line current from which the rate of harmonic distortion of 4,6% and power factor of 0.999 was obtained. In this case the waveform of the line voltage from which the reference current is generated presents a distortion rate of 2.9%.

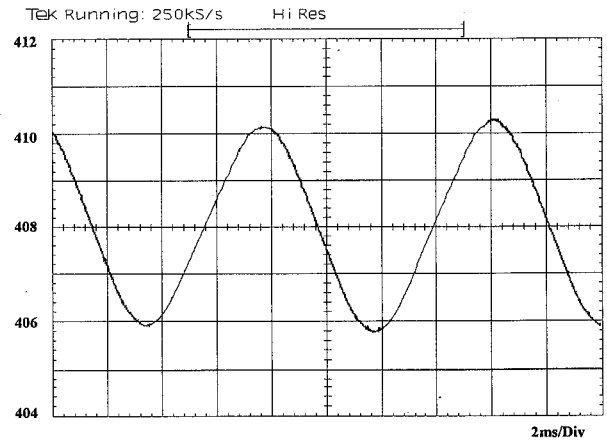


Fig. 14 - Capacitor C_0 voltage (V)

5. CONCLUSIONS

Based on the theoretical study and design procedure was projected the Zeta converter operating in continuous conduction mode applied in power factor correction. The experimental results obtained confirm the study presented.

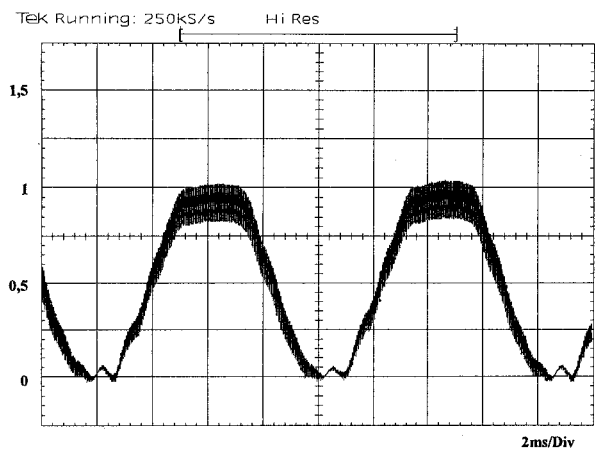


Fig. 15 - Inductor L_0 current (A)

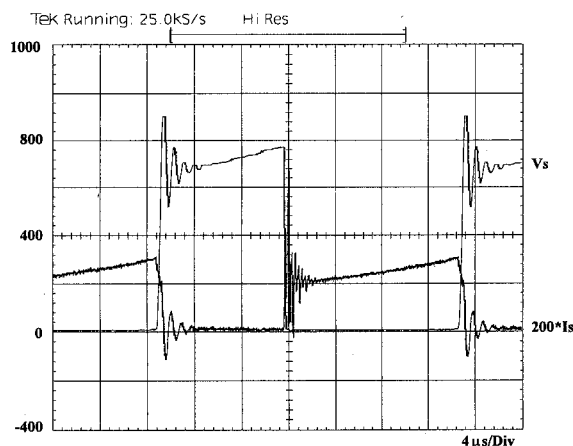


Fig. 16 - Switch voltage (V) and Current (A)

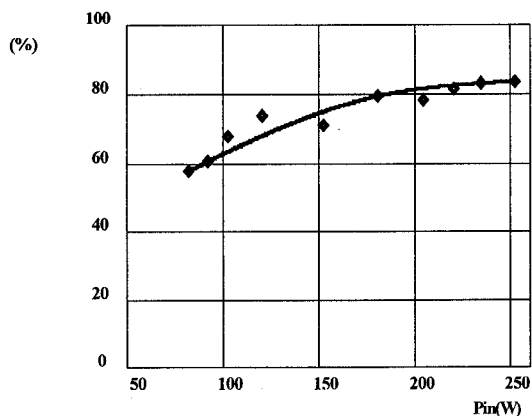


Fig. 17 - Efficiency

According to the results we have a structure with the following characteristics:

- It allows correction of power factor operating in continuous mode and therefore more adequate to the application in higher power;
- Naturally isolated;
- It operates either as step up or step down voltage;
- It can allow a regulated output voltage with only one power processing stage;

6. REFERENCES

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