

A NEW FAMILY OF ZVS-PWM ACTIVE-CLAMPING DC-TO-DC BOOST CONVERTERS: ANALYSIS, DESIGN, AND EXPERIMENTATION

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Abstract - The purposes of this paper is to introduce a new family of ZVS-PWM active-clamping DC-to-DC boost converters. This technique presents ZVS commutation without additional voltage stress and a significant increase in the circulating reactive energy throughout the converters. So, the efficiency and the power density become advantages when compared to the hard-switching boost converter. Thus, these converters may become very attractive in power factor correction applications. In this paper the complete family of boost converters is shown, and one particular circuit, taken as an example, is analyzed, simulated, and experimented. Experimental results are presented, taken from a laboratory prototype rated at 1600W, input voltage of 300V, output voltage of 400V, and operating at 100kHz. The measured efficiency at full load was 98%, and the converter kept an efficiency up to 95% from 17% to 100% of full load, without additional voltage and current stresses.

I. INTRODUCTION

The boost converter, as a preregulator, in AC-to-DC high power factor and low THD power supplies, has shown to be the best choice for single-phase rectification. Thus, this converter has played an important role in the power electronics area, and it has been the subject of incessant studies in the search of better efficiency and lower weigh and volume.

Through the synthesis technique of clamped mode DC-to-DC converters topologies, presented in [01], it was possible to generate six different circuits of boost converters. These circuits are presented and studied hereafter.

Figure 1 shows the six boost converters. In all of them the power transferred to the load is by a boost stage, while the clamping action is by a buck stage, shown in Figure 1.a, a boost stage in Figure 1.b, a buck-boost stage in Figure 1.c, a Cuk stage in Figure 1.d, a SEPIC stage in Figure 1.e, and a zeta stage in Figure 1.f. So, these converters will be called by Boost-buck, Boost-boost, Boost-buck-boost, Boost-cuk, Boost-sepic and Boost-zeta.

These converters differ from a conventional Boost PWM converter by an additional auxiliary switch (S_2), one or two

resonant inductors (L_{r1} , L_{r2}), a resonant capacitor (C_r), which includes the output capacitance of the power switches, and one or two clamping capacitors (C_{c1} , C_{c2}). Where, S_1 is the main switch.

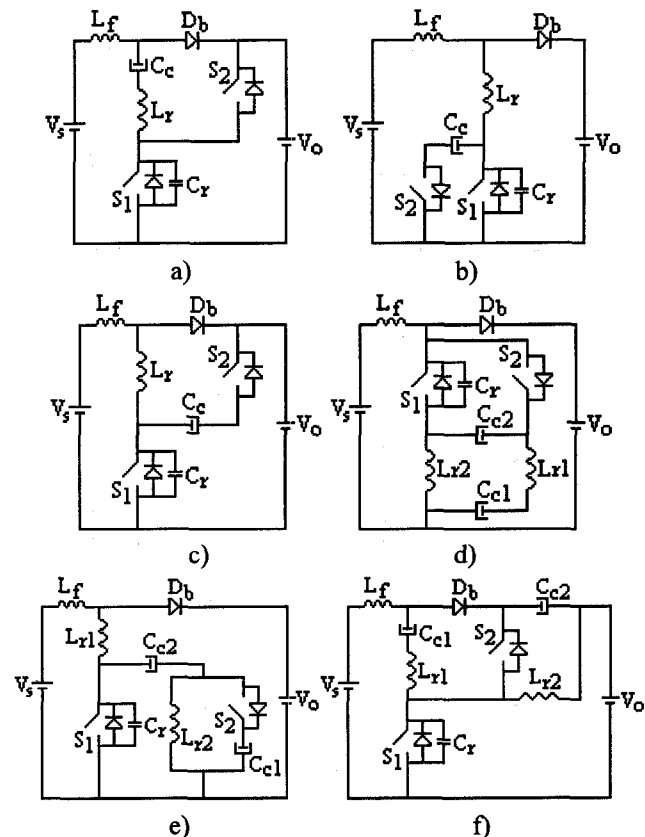


Fig. 1. ZVS-PWM active-clamping boost converters: a) Boost-buck; b) Boost-boost; c) Boost-buck-boost; d) Boost-cuk; e) Boost-sepic; f) Boost-zeta.

II. OPERATION AND ANALYSIS OF THE BOOST-BUCK-BOOST

A. Principle of Operation

To simplify the analysis, the input filter inductance is assumed large enough to be considered as a current source (I_s). The capacitor (C_c) is selected to have a large

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capacitance so that the voltage V_c across the capacitor C_c could be considered as a constant one. The six topological stages and key waveforms of the Boost-buck-boost converter to one switching cycle, are shown in Figure 2 and 3. In those Figures it can be seen that the two switches are switched in a complementary way. The main switch (S_1) is turned off at $t=t_0$, when the switching period starts.

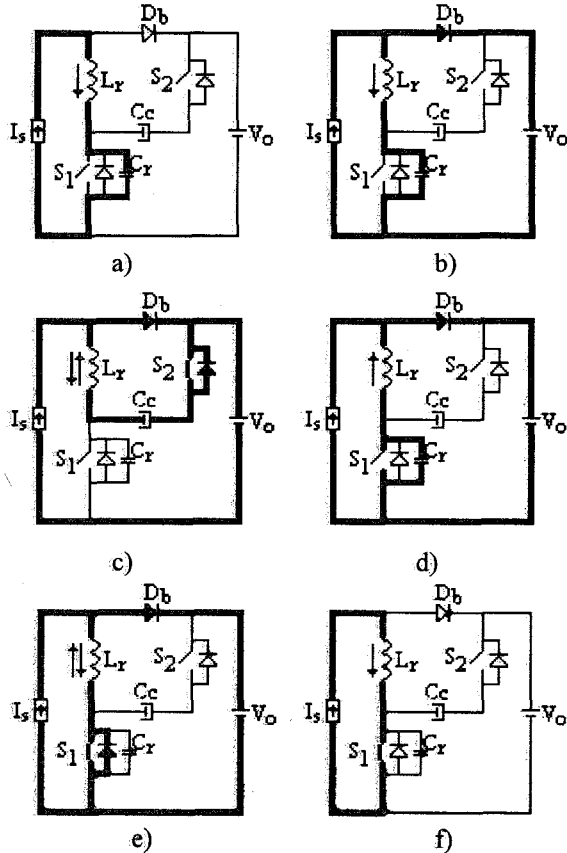


Fig. 2. Topological stages assumed by Boost-buck-boost converter.

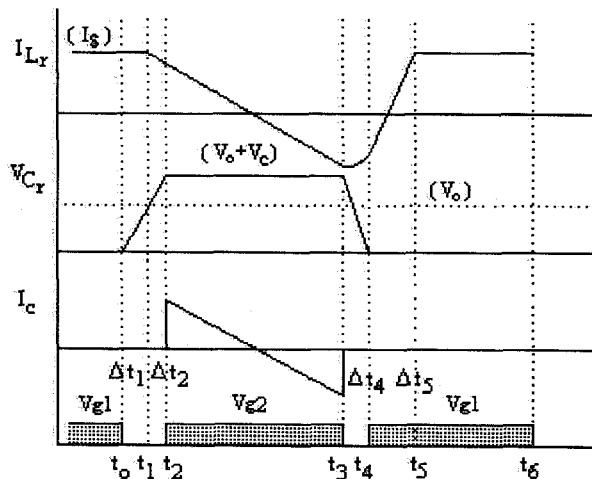


Fig. 3. Relevant ideal waveforms.

Prior to t_0 , the main switch (S_1) is on and the auxiliary switch is off. When S_1 is turned off, at $t=t_1$, the capacitor C_r is linearly charged, by I_s , to V_0 . Due to the presence of C_r , S_1 is turned off with no switching loss. Then V_{Cr} reaches V_0 , the boost diode (D_b) starts conducting. The current through L_r and V_{Cr} evolves in a resonant way, and V_{Cr} rises from V_0 up to V_c+V_0 . After that, the voltages are clamped. As $V_{Cr}(t)=V_c+V_0$, the voltage across S_2 is zero, thus S_2 turns on with no losses (ZVS). The L_r current ramps down until it reaches zero, when it changes its direction and rises again. This stage ends when S_2 is turned off at $t=t_3$. The voltage across C_r falls, due to the resonance between L_r and C_r , until it reaches zero at $t=t_4$. In stage 5, S_1 is turned on with no switching losses (ZVS), because V_{Cr} became null. The current through L_r changes its polarity and ramps up to reaches I_s . At $t=t_5$, the diode D_b becomes reversibly biased and power is not transferred to the load. This stage ends when S_1 is turned off at the end of the switching cycle.

B. DC voltage conversion ratio and DC voltage clamping ratio

As the time intervals Δt_1 , Δt_2 and Δt_4 are very short, in relation to the switching cycle, they will not be considered in this analysis. Thus, let us consider the waveform shown in Figure 4.

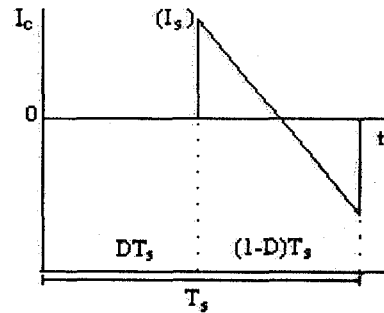


Fig. 4. Current through C_c .

The power that flows in the clamping capacitor must be zero in a switching cycle, for the operation to be steady. The voltage across C_c is constant, so its average current must be zero. Thus:

$$\int_0^{(1-D)T_s} \left[\frac{-V_c}{L_r} t + I_s \right] dt = 0 \quad (01)$$

then,

$$\beta = \frac{V_c}{V_0} = \frac{2L_n}{(1-D)} \quad (02)$$

$$\frac{V_{Spk}}{V_0} = \beta + 1 = 1 + \frac{2L_n}{(1-D)} \quad (03)$$

$$q = \frac{V_0}{V_s} = \frac{1}{1 - [D - 2L_n]} \quad (04)$$

where:

$$L_n = L_r \frac{I_s}{V_0 T_s} = L_r \frac{I_0}{V_s T_s} \quad (05)$$

and, V_{Spk} is the maximum voltage across S_1 and S_2 . The DC voltage clamping ratio given by (03), is graphically represented in Figure 5.a, and the DC voltage conversion ratio (q), is shown in Figure 5.b, for different duty cycles (D).

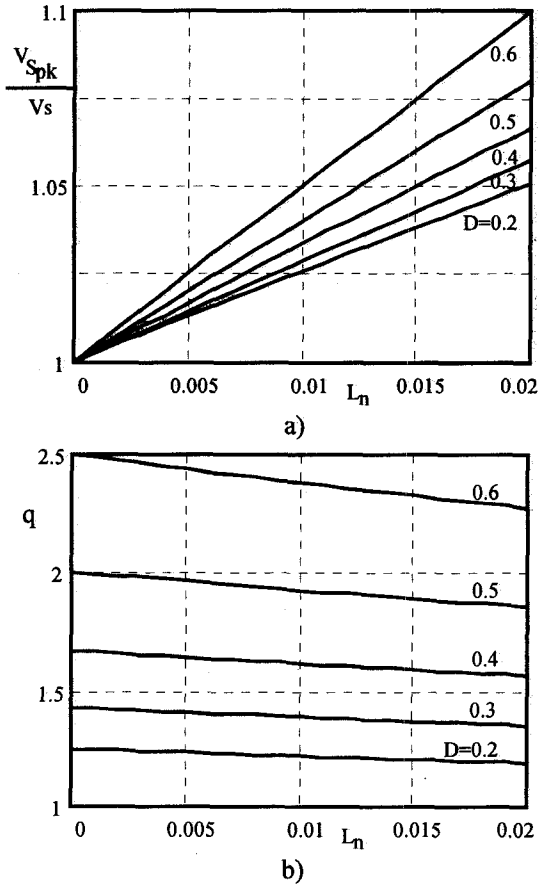


Fig. 5. Boost-boost, Boost-buck-boost, Boost-cuk, and Boost-sepic: a) theoretical dc voltage clamping ratio across switches ; b) theoretical dc voltage conversion ratio.

C. Commutation Analysis

Due to the capacitance C_r , S_1 and S_2 are turned off with no losses, in a ZVS way. However, S_1 and S_2 will turn on with no losses, only if there is enough energy stored in L_r to achieve soft commutation. At $t=t_1$, it is necessary to charge C_r from V_0 to V_c . At $t=t_3$, it is necessary to discharge C_r from V_c+V_0 to zero. The latter is more difficult because it needs more energy. Thus, if enough energy is guaranteed to achieve soft commutation for S_1 , then S_2 will achieve soft

commutation too. Thus, from energy relationships in L_r and C_r , at $t=t_3$, we have:

$$L_n \geq \frac{(1-D)}{(1-D)f - 2} \quad (06)$$

where,

$$f = \frac{f_0}{f_s} \quad (07)$$

As that result was achieved on a model with imposed current, then, at $t=t_3$, the current through L_r is equal to the average input current. But, in the real prototype, there is an input inductor that has maximum current greater than average current, so there is more energy stored to commutation. Thus, equation (06) must have a correction factor, which is represented in equation (08).

$$L_{n_{min}} = \frac{1}{\pi f(2+r) - \frac{2}{(1-D)}} \quad (08)$$

Where, (r) is the percentage input current ripple.

$$r = \frac{\Delta I_s}{I_s} \quad (09)$$

and, if the efficiency were considered, the expression becomes:

$$L_{n_{min}} = \frac{\eta}{\pi f(2+r) - \frac{2}{(1-D)}} \quad (10)$$

From the analysis before, it is clear that soft-commutation, when S_1 turns on, will be achieved depending on I_s and L_r . And, as I_s depends on the processed power, then that commutation will occur with no losses, only in a range of load that will be established through equation (08). But although that commutation is not completely without losses, the converter will still operate with high efficiency in light load situations, because there will always be enough energy stored in L_r to help the commutation process, and the lost energy never will be so high, as in a completely hard commutation.

As the critical commutation is when S_1 turns on, it is important to determine the time interval between the turning on of S_1 and turning off of S_2 . This time interval is necessary for the existence of soft commutation. Then:

$$t_d = \frac{(V_0 + V_c)}{2I_s} C_r + \frac{I_s}{2V_0} L_r \quad (11)$$

D. Voltage and current stresses on switches

Below, are presented the voltage and current stresses on switches. All current and voltages are normalized in relation to I_s and V_0 .

	Switch S_1	Switch S_2	Diode D_b
V_{max}	$1 + \frac{2L_n}{(1-D)}$	$1 + \frac{2L_n}{(1-D)}$	1
I_{pk}	1	1	2
I_{rms}	$\sqrt{D - \frac{4}{3}L_n}$	$\sqrt{\frac{(1-D)}{3}}$	$\sqrt{\frac{2}{3}(1-D) + 4L_n}$
I_{avg}	$D - L_n$	0	$1 - (D - L_n)$

Tab. 1. Current and voltage stresses on switches for Boost-buck-boost converter.

III. RELEVANT ANALYSIS RESULTING FROM THE ENTIRE FAMILIES OF CONVERTERS

All the converters were analyzed and it was possible to arrive at some conclusions by comparing their performances. Shown below, in Figures 6 and 7, are the dc voltage clamping ratios across the switches and the dc voltage conversion ratio, for Boost-buck and Boost-zeta converters, while the other converters, are shown in Figure 5.

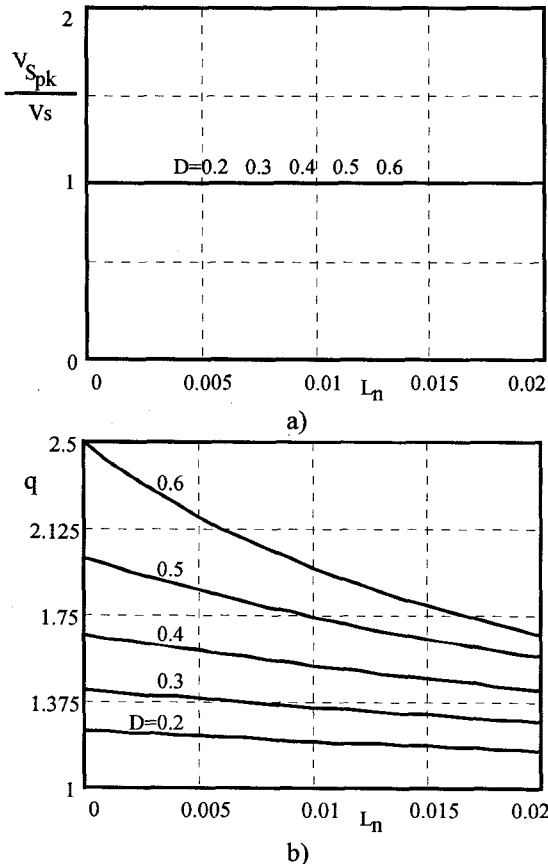


Fig. 6. Boost-buck converter: a) theoretical voltage clamping ratio across switches; b) theoretical output characteristics.

Although the Boost-boost, Boost-buck-boost, Boost-cuk, and Boost-sepic converters present the same external characteristics and the same voltage clamping on switches, conceptually they are different, and present different voltages across the clamping capacitor.

Through the analysis it was proved that the Boost-buck converter presented lower voltage stress on switches, but higher current stress, and its clamping capacitor is under all load current, which is a disadvantage. The Boost-zeta converter presented the worst performance, because has higher current and voltage stresses on switches, and less efficiency than the others.

From that analysis, one can conclude that the buck-boost clamping action, is the best for Boost converters applications.

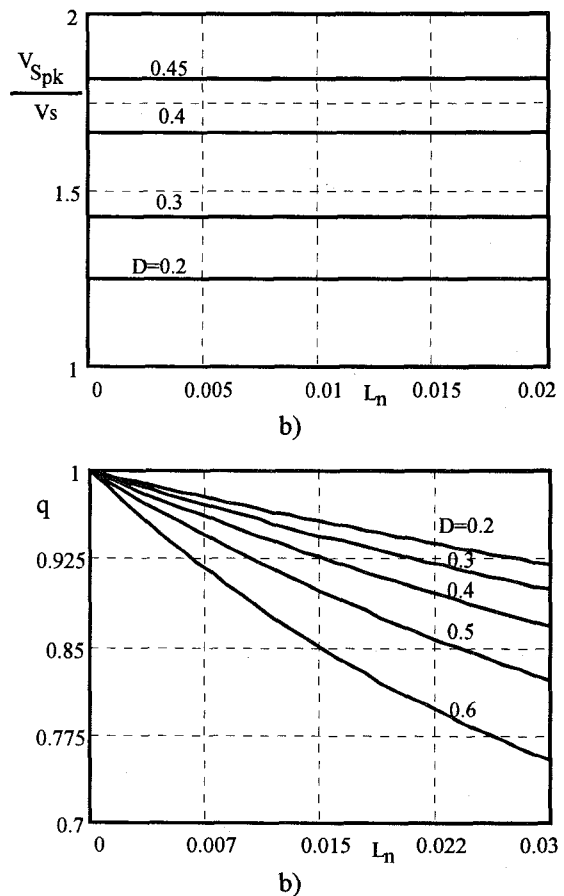


Fig. 7. Boost-zeta converter: a) theoretical voltage clamping ratio across switches; b) theoretical output characteristics.

IV. DESIGN EXAMPLE

In this section, a design example for the Boost-buck-boost converter will be presented. The specifications are as follows:

$$V_s=300V \text{ (input voltage); } V_0=400V \text{ (output voltage); } P_{out}=1600W \text{ and } f_s=100kHz.$$

The efficiency must be kept high from light load conditions to full load. Therefore, the load range with soft commutation in the main switch (S_1) will be established from 55% to 100% of full load. From the specifications it is possible to achieve the DC voltage-conversion-ratio, given by:

$$q = \frac{V_0}{V_s} = \frac{400}{300} = 1.333$$

Throughout the DC voltage-conversion-ratio and the output characteristics, shown in Figure 5.b, are obtained the nominal duty cycle, the normalized resonant inductance and the resonant inductance. The determination of those parameters results in the establishment of the operation point, and in the range of load with soft commutation in S_1 . Although it is important to consider that the greater the value of L_r the greater will be the range of load with soft commutation in S_1 which results in greater clamping voltage. As a closed solution in this case would be difficult to achieve, it is necessary to do some interactions to obtain the desired operation point, and the range of load with soft commutation in S_1 . So, it is necessary to determine the values of D , L_n , L_r , and C_r , and then, to verify if the load of range with soft commutation in S_1 , is that desired. If it is less than that desired, the value of L_r must be increased. Then, with $q=1.333$, and choosing $D=0.302$, through Figure 5.b, it has $L_n=0.0519$, and from Figure 5.a, results:

$$\frac{V_{Spk}}{V_s} = 1.1487 \quad \beta = 0.1487$$

thus, we have:

$$L_r = \frac{L_n V_0}{f_s I_s} = 37\mu\text{H}$$

The resonant frequency, of the circuit L_r and C_r , must be much higher than the switching frequency so the commutations become a small part of the switching period. Then, $f=5.28$ has been chosen. So,

$$2\pi f_0 = \frac{1}{\sqrt{L_r C_r}} \Rightarrow C_r = 2.46\text{nF}$$

As the input current ripple is taken by 24% of the average input current, and the efficiency is considered as 95%, this results in:

$$L_{n_{min}} = \frac{0.95}{\pi \cdot 5.28 \cdot (2 + 0.24) - \frac{2}{(1 - 0.302)}} = 0.027645$$

Then, as $L_{n_{min}}=0.5327L_n$, a range of load with soft commutation in S_1 from 53.27% to 100% of full load is

obtained, which satisfy the specified value (from 55% to 100%).

The time interval between the turning on of S_1 and the turning off of S_2 is:

$$t_d = \left[\frac{0.45948}{2 \cdot 5.61} \cdot 2.46 + \frac{5.61 \cdot 37 \cdot 10^{-6}}{2 \cdot 400} \right] 10^{-6} \cong 360\text{ns}$$

V. EXPERIMENTAL RESULTS

Following the same design outlined in the preceding section, a Boost ZVS-PWM converter with clamping action buck-boost (Boost-buck-boost) was implemented, with the following specifications:

- output power $P=1600\text{W}$;
- input voltage $V_s=300\text{V}$;
- output voltage $V_0=400\text{V}$;
- switching frequency $f_s=100\text{kHz}$.

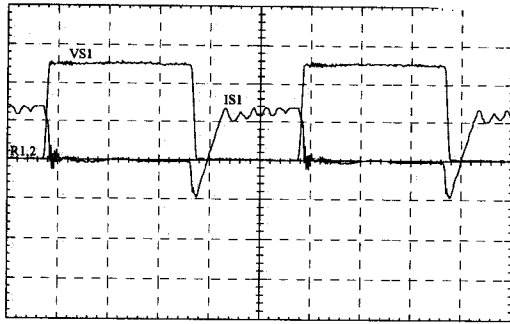
The power stage consists of the following parameters:

- switches S_1 and S_2 : Power MOSFET's APT5025;
- diode D_b : APT60D60;
- extern resonant capacitor C_{rext} : 1000pF/1.6kV;
- clamping capacitor C_c : 2.2 μF /200V;
- output filter capacitor C_f : 100 μF /250V;
- resonant inductor L_r : 37 μH , core (E-45/15)-Thornton;
- input filter inductor L_f : 600mH, core (E-55) Thornton.

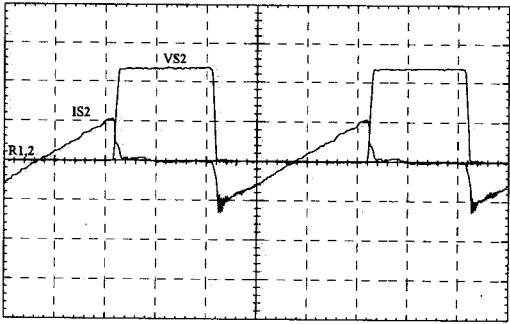
Experimentally obtained waveforms of the switches current and drain-to-source voltages are shown in Figure 8. The resonant inductor current and voltage across the resonant capacitor are shown in Figure 9.a, while the current through the diode D_b and the voltage across that diode are shown in Figure 9.b. These waveforms agree with those predicted theoretically, and as can be noted from the waveforms shown in Figure 8, the main switches (S_1 and S_2) present ZVS commutation and its voltages are clamped at a specified value.

The load range with integral soft commutation in S_1 , obtained experimentally, was from 48.5% to 100% of full load. In Figures 10 and 11, are shown the main waveforms with 48.5% of full load. As we can see, integral soft commutation is obtained for both switches S_1 and S_2 . For loads less than 48.5% of full load, S_1 will start to turn on with some losses, but the level of energy evolved in that commutation will be very low, which will not affect significantly the converter efficiency. Then, as S_2 will always switch without losses the converter will operate with high efficiency, even in light load situations.

The complete circuit diagram of the converter is shown in Figure 12.

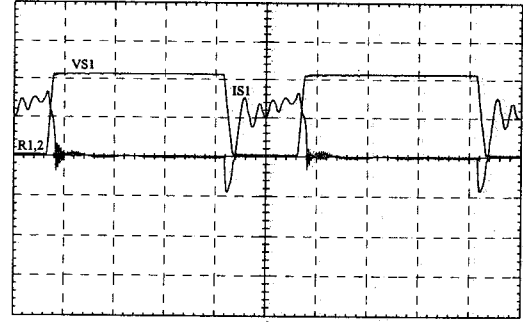


a)

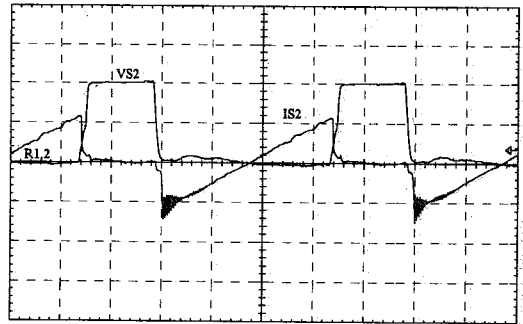


b)

Fig. 8. a) Drain-to-source voltage across S_1 and current through S_1 and C_r ; b) drain-to-source voltage across S_2 and current through S_2 ; (voltage: 200V/div; current: 5A/div; time scale: 2 μ s/div).

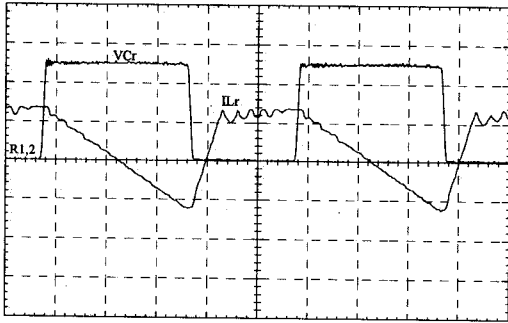


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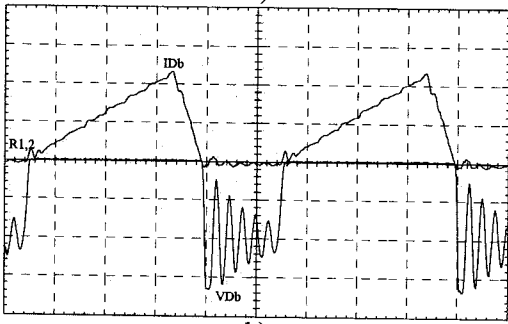


b)

Fig. 10. a) Drain-to-source voltage across S_1 and current through S_1 and C_r ; b) drain-to-source voltage across S_2 and current through S_2 ; (voltage: 200V/div; current: 2A/div; time scale: 2 μ s/div).

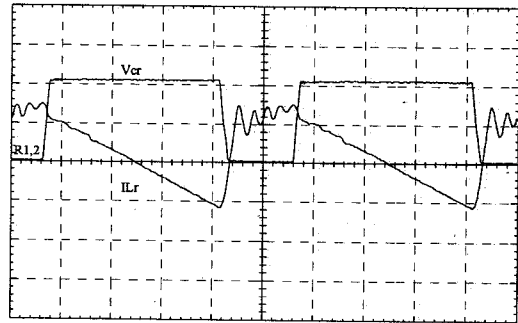


a)

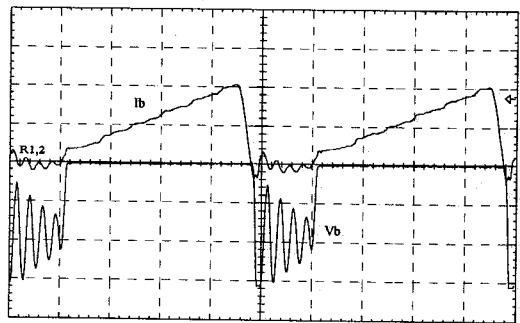


b)

Fig. 9. a) Voltage across C_r and current through L_r ; b) voltage across D_b and current through D_b ; (voltage: 200V/div; current: 5A/div; time scale: 2 μ s/div).



a)



b)

Fig. 11. a) Voltage across C_r and current through L_r ; b) voltage across D_b and current through D_b ; (voltage: 200V/div; current: 2A/div; time scale: 2 μ s/div).

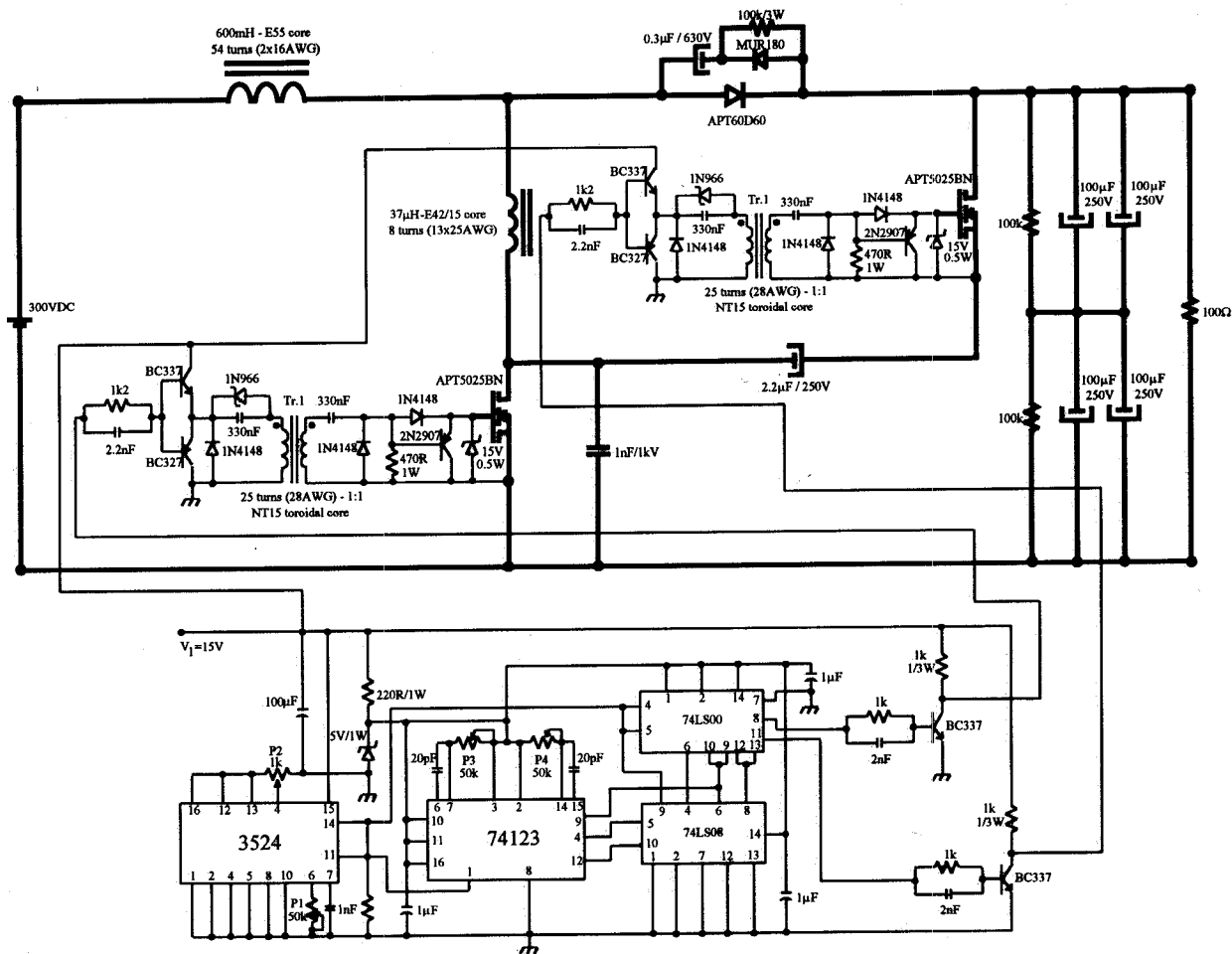


Fig. 12. Complete circuit of the implemented prototype.

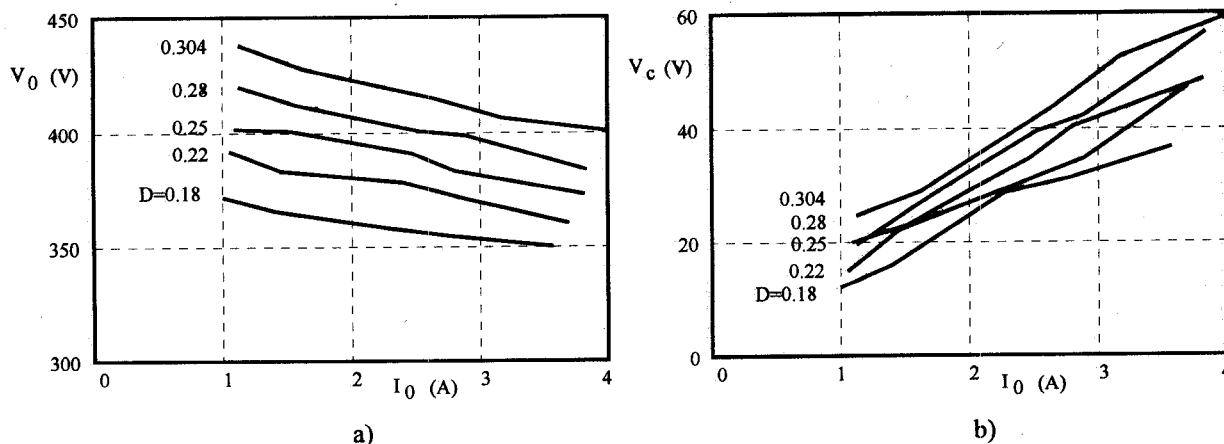


Fig. 13. a) Output voltage with different load conditions and duty cycle; b) voltage across the clamping capacitor with different load conditions and duty cycle.

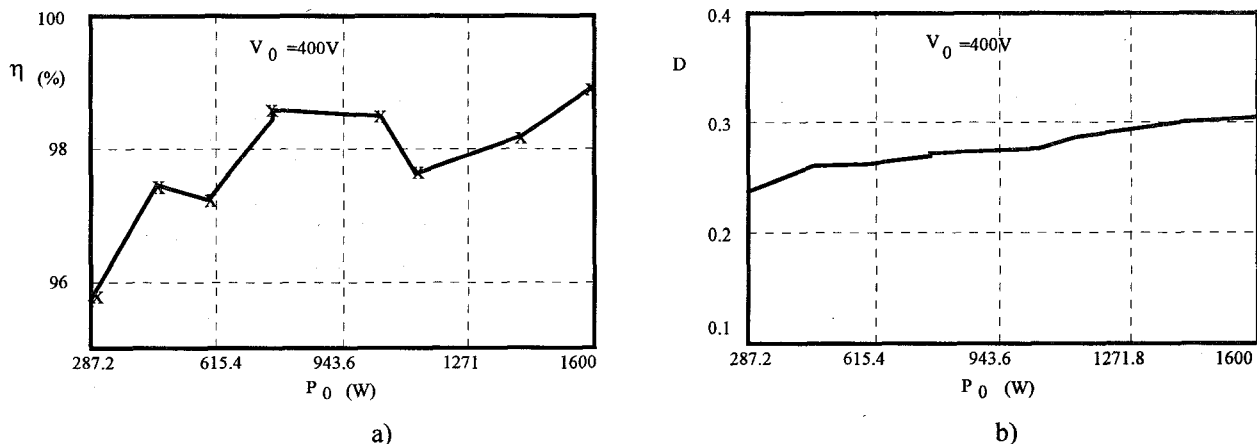


Fig. 14. a) Experimental efficiency curve with constant output and input voltage; b) duty cycle variation to keep output voltage constant with different load conditions.

In Figure 13.a, the output voltage as a function of output current is shown, for different duty cycles, and in Figure 13.b, the voltage across clamping capacitor for the same conditions can be noted.

The experimental efficiency curve of the converter, is shown in Figure 14.a, while the duty cycle necessary to keep the output voltage in 400V, is shown in Figure 14.b. The converter presented high efficiency (up to 95%) from 17.95% to 100% of full load.

VI. CONCLUSION

This paper presented a new family of ZVS-PWM Active-Clamping DC-to-DC Boost Converters. The Boost with clamping action buck-boost, Boost-buck-boost, converter was analyzed as an example. Theoretical studies and experimental results, allow us to draw the following conclusions:

- soft-commutation (ZVS) is achieved for the active switches without notable voltage and current stresses;
- the converters are regulated by the conventional PWM technique, at constant frequency;
- high efficiency was obtained from light load to full load.

The new converters are suitable for power factor correction rectifiers, particularly for 1.6kW power supplies, where MOSFET's can be used without increasing of conduction losses.

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