

A New ZVS-PWM Active-Clamping High Power Factor Rectifier: Analysis, Design, and Experimentation

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Abstract - In this paper is introduced a new single-phase rectifier, which features high power factor, regulation by conventional PWM technique, ZVS commutation and clamping action in both switches, and instantaneous average line current control. This rectifier consists of a front-end full-bridge diode rectifier followed by a ZVS-PWM, Buck-boost Active-Clamping, Boost converter. Experimental results are presented, taken from a laboratory prototype rated at 1.6kW, input ac voltage of 220Vrms, output dc voltage of 400V, and operating at 100kHz. The measured efficiency at full load was 95%.

I. INTRODUCTION

The most popular method to achieve high power factor and low line harmonics content consists of a front-end full-bridge diode rectifier followed by a boost converter. The main difficulty of this technique are the switching losses, which limit the maximum efficiency and switching frequency of the converter and consequently its minimum weigh and volume.

To overcome this disadvantage, several techniques featuring soft-switching have been proposed, to replace the hard-switching boost converter.

To achieve ZVS commutation and PWM modulation in a boost converter, it is necessary to employ an auxiliary switch, and sometimes with the increasing of voltage stress on switches.

The most known technique featuring ZVS commutation and PWM modulation for this application [1] presents ZVS commutation only in the main switch.

In this paper is proposed to replace the conventional hard-switching boost converter with a ZVS-PWM, buck-boost active-clamping, Boost converter [2, 3]. This converter presents ZVS commutation in both switches, without significant increasing in circulating energy inside the converter.

II. THE PWM-ZVS, BUCK-BOOST CLAMPING-ACTION, BOOST CONVERTER

This converter differs from a conventional Boost PWM converter by an additional auxiliary switch (S_2), a resonant inductor (L_r), a resonant capacitor (C_r), which includes the

output capacitance of the power switches, and a clamping capacitor (C_c), where, S_1 is the main switch. The circuit of this converter is shown in Figure 1.

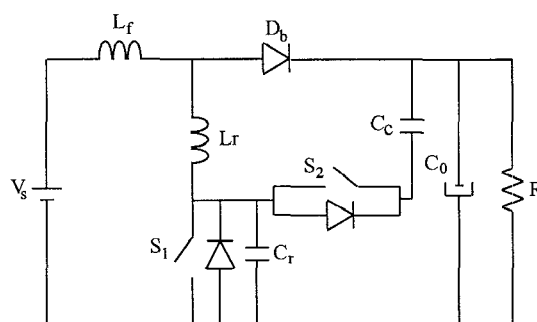


Fig. 1. ZVS-PWM, buck-boost active-clamping, boost converter.

A. Principle of Operation

To simplify the analysis, the input filter inductance is assumed large enough to be considered as a current source (I_s). The capacitor (C_c) is selected to have a large capacitance so that the voltage V_c across the capacitor C_c could be considered as a constant one. The six topological stages and key waveforms of the Boost-buck-boost converter to one switching cycle, are shown in Figure 2 and 3. In those Figures it can be seen that the two switches are switched in a complementary way. The main switch (S_1) is turned off at $t=t_0$, when the switching period starts.

Prior to t_0 , the main switch (S_1) is on and the auxiliary switch is off. When S_1 is turned off, at $t=t_0$, the capacitor C_r is linearly charged, by I_s , to V_0 . Due to the presence of C_r , S_1 is turned off with no switching loss. Then V_{Cr} reaches V_0 , the boost diode (D_b) starts conducting. The current through L_r and V_{Cr} evolves in a resonant way, and V_{Cr} rises from V_0 up to V_c+V_0 . After that, the voltages are clamped. As $V_{Cr}(t)=V_c+V_0$, the voltage across S_2 is zero, thus S_2 turns on with no losses (ZVS). The L_r current ramps down until it reaches zero, when it changes its direction and rises again. This stage ends when S_2 is turned off at $t=t_3$. The voltage across C_r falls, due to the resonance between L_r and C_r , until it reaches zero at $t=t_4$. In stage 5, S_1 is turned on with no switching losses (ZVS), because V_{Cr} became null. The

current through L_r changes its polarity and ramps up to reaches I_s . At $t=t_5$, the diode D_b becomes reversibly biased and power is not transferred to the load. This stage ends when S_1 is turned off at the end of the switching cycle.

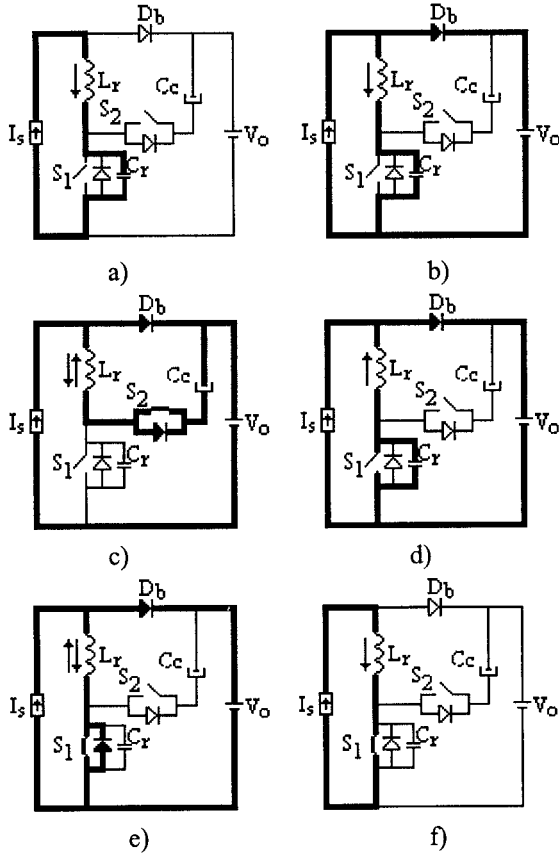


Fig. 2. Topological stages assumed by Boost-buck-boost converter in one switching cycle.

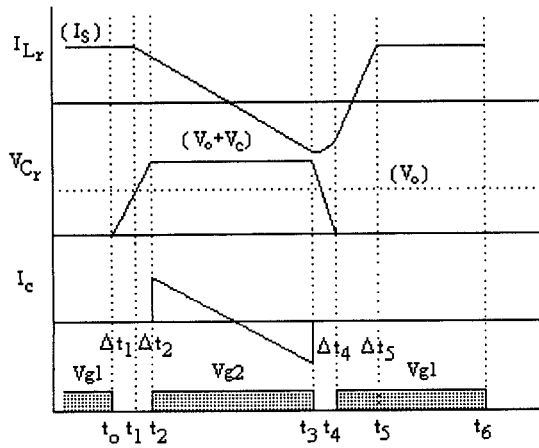


Fig. 3. Relevant ideal waveforms for one switching cycle.

B. DC voltage conversion ratio and DC voltage clamping ratio

As the time intervals Δt_1 , Δt_2 and Δt_4 are very short, in relation to the switching cycle, they will not be considered in this analysis. Thus, let us consider the waveform shown in Figure 4.

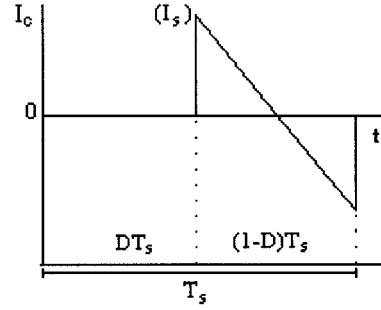


Fig. 4. Current through C_c for one switching cycle.

The power that flows in the clamping capacitor must be zero in a switching cycle, for the operation to be steady. The voltage across C_c is constant, so its average current must be zero. Thus:

$$\int_0^{(1-D)T_s} \left[\frac{-V_c}{L_r} t + I_s \right] dt = 0 \quad (01)$$

then,

$$\beta = \frac{V_c}{V_0} = \frac{2L_n}{(1-D)} \quad (02)$$

$$\frac{V_{S_{pk}}}{V_0} = \beta + 1 = 1 + \frac{2L_n}{(1-D)} \quad (03)$$

$$q = \frac{V_0}{V_s} = \frac{1}{1 - [D - 2L_n]} \quad (04)$$

where:

$$L_n = L_r \frac{I_s}{V_0 T_s} = L_r \frac{I_0}{V_s T_s} \quad (05)$$

and, $V_{S_{pk}}$ is the maximum voltage across S_1 and S_2 .

C. Current and voltage stresses on switches

In Table I are presented the voltage and current stresses on switches. All current and voltages are normalized in relation to I_s and V_0 .

Tab. 1. Current and voltage stresses on switches for Boost-buck-boost converter.

	Switch S_1	Switch S_2	Diode D_b
V_{\max}	$1 + \frac{2L_n}{(1-D)}$	$1 + \frac{2L_n}{(1-D)}$	1
I_{pk}	1	1	2
I_{rms}	$\sqrt{D - \frac{4}{3}L_n}$	$\sqrt{\frac{(1-D)}{3}}$	$\sqrt{\frac{2}{3}(1-D) + 4L_n}$
I_{avg}	$D - 2L_n$	0	$1 - (D - 2L_n)$

D. Commutation Analysis

Due to the capacitance C_r , S_1 and S_2 are turned off with no losses, in a ZVS way. However, S_1 and S_2 will turn on with no losses, only if there is enough energy stored in L_r to achieve soft commutation. At $t=t_1$, it is necessary to charge C_r from V_0 to V_c . At $t=t_3$, it is necessary to discharge C_r from V_c+V_0 to zero. The latter is more difficult because it needs more energy. Thus, if enough energy is guaranteed to achieve soft commutation for S_1 , then S_2 will achieve soft commutation too. Thus, from energy relationships in L_r and C_r , at $t=t_3$, we have:

$$L_n \geq \frac{(1-D)}{(1-D)f - 2} \quad (06)$$

where,

$$f = \frac{f_0}{f_s} \quad (07)$$

As that result was achieved on a model with imposed current, then, at $t=t_3$, the current through L_r is equal to the average input current. But, in the real prototype, there is an input inductor that has maximum current greater than average current, so there is more energy stored to commutation. Thus, equation (06) must have a correction factor, which is represented in equation (08).

$$L_{n_{\min}} = \frac{1}{\pi f(2+r) - \frac{2}{(1-D)}} \quad (08)$$

Where, (r) is the percentage input current ripple,

$$r = \frac{\Delta I_s}{I_s} \quad (09)$$

and, if the efficiency were considered, the expression becomes:

$$L_{n_{\min}} = \frac{\eta}{\pi f(2+r) - \frac{2}{(1-D)}} \quad (10)$$

From the analysis before, it is clear that soft-commutation, when S_1 turns on, will be achieved depending on I_s and L_r . And, as I_s depends on the processed power, then that commutation will occur with no losses, only in a range of load that will be established through equation (08). But although that commutation is not completely without losses, the converter will still operate with high efficiency in light load situations, because there will always be enough energy stored in L_r to help the commutation process, and the lost energy never will be so high, as in a completely hard commutation.

As the critical commutation is when S_1 turns on, it is important to determine the time interval between the turning on of S_1 and turning off of S_2 . This time interval is necessary for the existence of soft commutation. Then:

$$t_d = \frac{(V_0 + V_c)}{2I_s} C_r + \frac{I_s}{2V_0} L_r \quad (11)$$

III. BOOST BUCK-BOOST CONVERTER IN HIGH POWER FACTOR RECTIFIER APPLICATION WITH AVERAGE CURRENT CONTROL

The Unitrode PFC controller, UC3854 [4], was employed. It was possible because the converter operates in continuous current mode with constant switching frequency. This approach differs of the conventional one, usual PFC boost converters, by the presence of a bootstrap and a dead-time circuits necessary to drive the auxiliary switch.

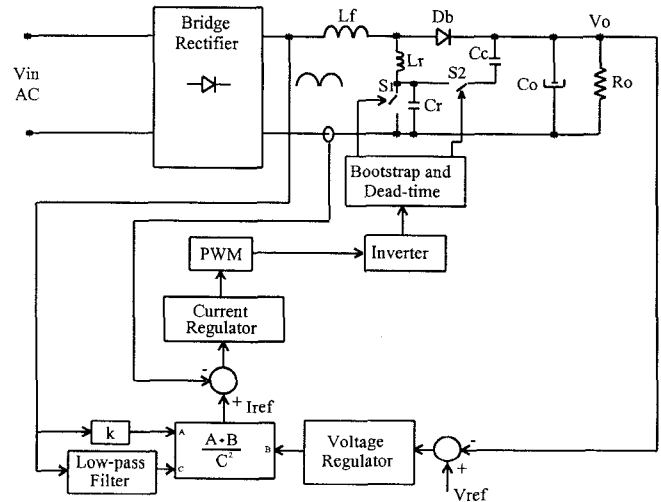


Fig. 5. Complete block diagram of the PFC Boost buck-boost converter.

The International Rectifier IR2111 driver was chosen, because it is a MOSFET gate driver, which features a floating supply designed for bootstrap operation with a dead-time of 450ns typical. The block diagram of the complete circuit is shown in Figure 5.

A. Theoretical Analysis

In a switching cycle, the operation of Boost buck-boost converter, in the AC-DC mode, is the same as in DC-DC mode, although it is necessary to watch that the converter will operate with a input voltage senoidal and duty-cycle will be adjusted to keep constant output voltage with input current senoidal and in phase with input voltage. So, in the AC-DC mode, input voltage and current are rectified senoidal waveforms, then we have:

$$V_s(\theta) = V_{spk} \sin \theta \quad \text{and} \quad I_s(\theta) = I_{spk} \sin \theta \quad (12)$$

where:

$$\theta = \omega t \quad \text{and} \quad \omega t = 2\pi 120 \quad (13)$$

Then,

$$L_n(\theta) = \frac{L_r I_{spk}}{V_0 T_s} \sin \theta \quad \text{or} \quad L_n(\theta) = L_{n1} \sin \theta \quad (14)$$

Then, re-writing (04) for AC-DC mode,

$$\frac{V_0}{V_{spk} \sin \theta} = \frac{1}{1 - [d(\theta) - 2L_n(\theta)]} \quad (15)$$

Defining,

$$q_1 = \frac{V_{spk}}{V_0} \quad (16)$$

results:

$$d(\theta) = 1 + (2L_{n1} - q_1) \sin \theta \quad (17)$$

From (17) it is possible to Know how duty-cycle vary in an input voltage half cycle. It is shown in Figure 6.

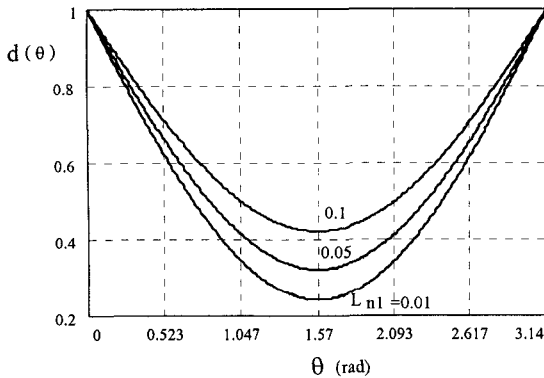


Fig. 6. Duty-cycle variation.

B. Resonant Parameters

The resonant parameters are given in function of the desired range width, in an input voltage cycle, with ZVS turn on in S_1 .

Then, from a desired range width (δ), in radian, it is possible to determine θ_1 , as following:

$$\theta_1 = \frac{\pi - \delta}{2} \quad (18)$$

In the same way, as in DC-DC mode, from (06) we have:

$$L_{n1} \geq \frac{q_1}{4} \left[1 - \sqrt{1 - \frac{4}{\pi q_1 f \sin \theta_1}} \right] \quad (19)$$

Figure 7 shows L_{n1} minimum as a function of θ_1 .

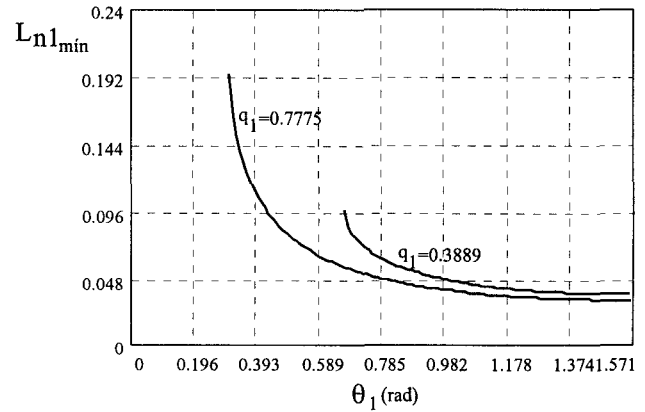


Fig. 7. L_{n1} minimum as a function of θ_1 .

Then, from (14) and (19), it is possible to determine the resonant inductance. Thus, it results:

$$L_r = \frac{L_{n1} V_0 T_s}{I_{spk}} \quad (20)$$

And the resonant capacitance is given by:

$$f = \frac{f_0}{f_s} \Rightarrow C_r = \frac{1}{(2\pi f_s f)^2 L_r} \quad (21)$$

C. Input Inductance

From the same analysis it is not difficult to determine the input inductance, which is given by:

$$L_f = \frac{V_{spk}}{4(q_1 - 2L_{n1}) \Delta I_{max} f_s} \quad (22)$$

D. Voltage and current stresses on switches

From TABLE I, for AC-DC mode we have:

$$V_{S\max} = \left[1 + \frac{2L_{n1}}{(q_1 - 2L_{n1})} \right] V_0 \quad (23)$$

$$I_{S1\max} = I_{S2\max} = I_{\text{spk}} \quad (24)$$

$$I_{S1\text{rms}} = I_{\text{spk}} \sqrt{\frac{1}{2} + \frac{4}{3\pi} \left(\frac{2L_{n1}}{3} - q_1 \right)} \quad (25)$$

$$I_{S2\text{rms}} = I_{\text{spk}} \frac{2}{3} \sqrt{\frac{(q_1 - 2L_{n1})}{\pi}} \quad (26)$$

In Figure 8, the maximum clamping voltage across switches as a function of L_{n1} is shown, for an output voltage of 400V and input voltage of 220Vrms ($q_1=0.7775$) and 110Vrms ($q_2=0.3889$).

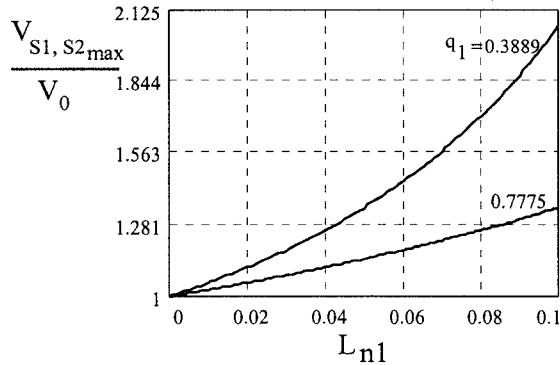


Fig. 8. Maximum clamping voltages across switches.

IV. SIMPLIFIED DESIGN EXAMPLE

In this section, a design example for the Boost-buck-boost converter will be presented. The specifications are as follows:

$$V_s = 220\text{Vrms (input voltage); } V_0 = 400\text{V (output voltage); } \\ P_{\text{out}} = 1600\text{W; } f_s = 100\text{kHz; } \eta = 95\%.$$

For the Boost-buck-boost converter, it is important to specify the operation range with integral soft commutation in the main switch (S_1). It will be established in 50% of the input voltage period. From the specifications it is possible to obtain q_1 . So, we have:

$$q_1 = \frac{V_{\text{spk}}}{V_0} = \frac{311}{400} = 0.7775$$

If we take,

$$f = \frac{f_0}{f_s} = 8$$

and,

$$\theta_1 = \frac{\pi - \delta}{2} = \frac{\pi - 0.5\pi}{4} = \frac{\pi}{4} \text{ rad}$$

Then,

$$L_{n1} \geq \frac{q_1}{4} \left[1 - \sqrt{1 - \frac{4}{\pi \cdot q_1 \cdot f \cdot \sin\theta}} \right] = 0.031$$

and,

$$L_r = \frac{L_{n1} \cdot V_0 \cdot T_s}{I_{\text{spk}}} = \frac{0.031 \cdot 400 \cdot 10 \cdot 10^{-6}}{10.83} = 11.5\mu\text{H}$$

Then, the resonant capacitance will be:

$$C_r = \frac{1}{(2\pi \cdot f_s \cdot f)^2 \cdot L_r} = 3.5\text{nF}$$

and, the input filter inductance is given by:

$$L_f = \frac{311}{4 \cdot (0.7775 - 2 \cdot 0.031) \cdot 2.17 \cdot 100 \cdot 10^{-3}} \cong 500\mu\text{H}$$

V. EXPERIMENTAL RESULTS

In order to experimentally verify the principle of operation and theoretical analysis, a 1.6 kW, 100kHz Boost-buck-boost high power factor converter has been implemented. The complete implemented circuit of the converter is shown in Figure 14. This prototype is regulated at 400V dc output with 220V ac input.

It is important to notice that the body diodes and parasitic capacitances of main MOSFET's are utilized. The power stage consists of the following parameters:

- switches S_1 and S_2 : Power MOSFET's IRFP460;
- diode D_b : APT30D60;
- external resonant capacitor C_{rext} : 1000pF/1.6kV;
- clamping capacitor C_c : 2.2μF/200V;
- output filter capacitor C_f : 100μF/250V;
- resonant inductor L_r : 37μH, core (E-45/15)-Thornton;
- input filter inductor L_f : 600mH, core (E-55) Thornton.

Experimentally obtained waveforms of input current and input voltage for the prototype operating at 1.6kW are shown in Figure 9. The input voltage presents some distortion, therefore the input current will be distorted too. The THD of the input voltage is about 3.4%. The power factor obtained for 1.6kW was 0.996 with a THD of 5.63% in the input current.

Current and drain-to-source voltages on switches are shown in Figure 10. These waveforms agree with those predicted theoretically, and as can be noted from the

waveforms shown in Figure 10, the main switches (S_1 and S_2) present ZVS commutation and its voltages are clamped at a specified value.

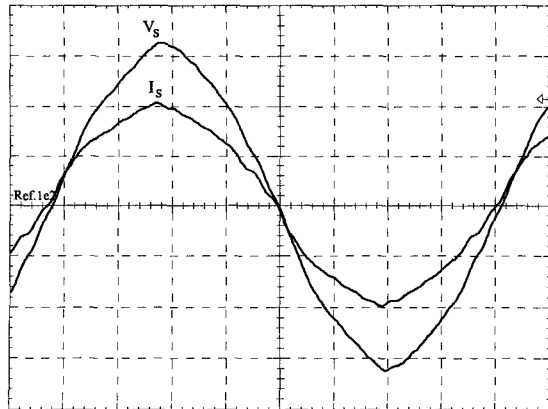
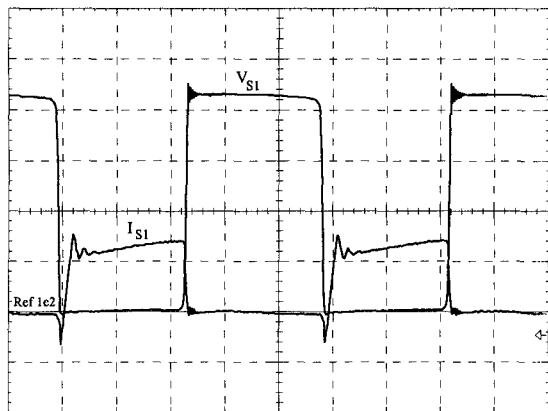


Fig. 9. Input voltage and input current. (voltage: 100V/div; current: 5A/div; time scale: 2ms/div).



a)



b)

Fig. 10. a) Drain-to-source voltage across S_1 and current through S_1 and C_r ; b) drain-to-source voltage across S_2 and current through S_2 ; (voltage: 100V/div; current: 5A/div; time scale: 2 μ s/div).

The harmonic distribution of input voltage and input current are shown in Figures 11 and 12.

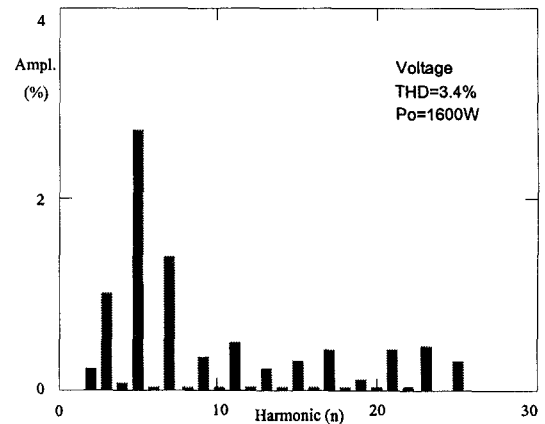


Fig. 11. Harmonic spectrum of input voltage.

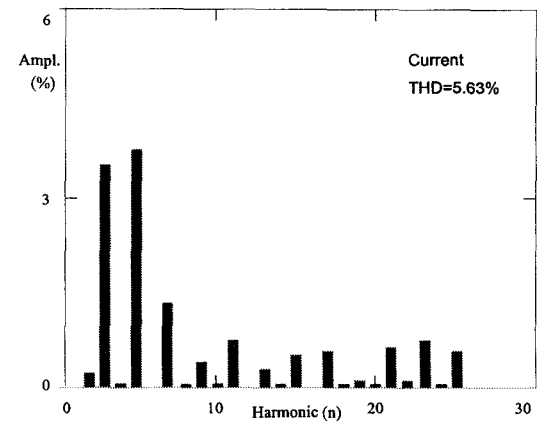


Fig. 12. Harmonic spectrum of input current.

The efficiency as a function of the output power is shown in Figure 13. The efficiency obtained at full load is 95%.

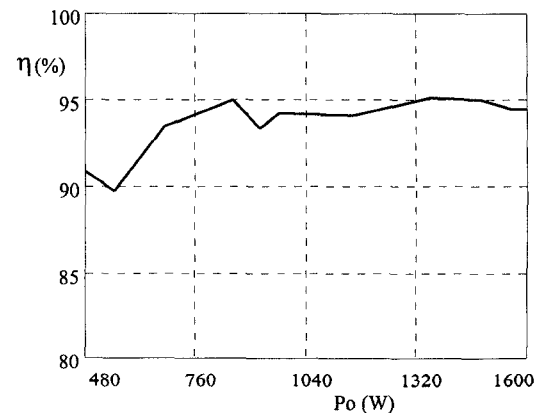


Fig. 13. Efficiency of the ZVS-PWM high power factor boost-buck-boost converter.

