

A NEW DC-TO-DC ZVS PWM CONVERTER FOR HIGH INPUT VOLTAGE APPLICATIONS

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Abstract - A new three-level DC-to-DC converter controlled by pulse-width modulation is proposed in this paper. This converter is suitable for high input voltage and high power applications featuring zero-voltage switching and half of the input voltage as the maximum voltage across the switches. The complete operating principle, theoretical analysis, relevant equations and design example are provided in this paper. The experimental results of a 1.5kW prototype, operating at 50kHz, rated at 600V input voltage and 25 A output current, are presented.

I. INTRODUCTION

On the design of high frequency switching mode power supplies for high power applications, the conventional full-bridge zero-voltage-switching pulse-width-modulation (FB-ZVS-PWM) converter [1] is considered one of the best alternatives. This converter possesses the most desirable characteristics of both the hard switching PWM and the soft switching converters, while avoiding their major drawbacks, such as commutation losses in the first group, and variable switching frequency and high conduction losses in the second group.

However, the conventional FB-ZVS-PWM converter is not suitable for high input voltage applications because the total input voltage is applied across its blocking switches.

Among the alternatives to overcome this drawback are: the series connection of switches and the use of multilevel topologies. In the series connection of the switches, the static and dynamic sharing of the voltage across the switches is difficult to obtain and requires specific techniques [1]. Multilevel topologies [2,3,4,5] seems to be a more effective solution because they can solve the problem of static and dynamic sharing of the voltage and reduces problems of EMI, once the dv/dt over the switches can be limited to standard values.

This paper presents the analysis, design procedure and experimental results of a three-level DC-DC converter shown in figure 1. This converter is controlled by pulse-width modulation (PWM) featuring ZVS commutation and half of the input voltage as the maximum voltage applied across the switches.

II. THE CIRCUIT AND PRINCIPLE OF OPERATION

A. Circuit Description

The converter presented in figure 1 consists in a cascade connection of the primary side of two half-bridge converters. One of the converters is formed by capacitors C_{i1} and C_{i2} , switches S_1 and S_4 and transformer Tr_2 . The other one is formed by capacitors C_{m1} and C_{m2} , switches S_2 and S_3 and transformer Tr_1 .

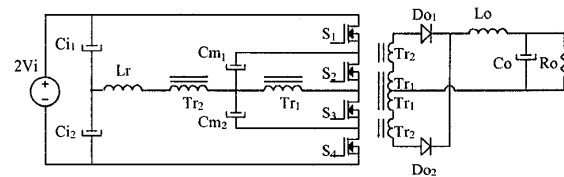


Fig. 1 – The proposed TL PWM DC-to-DC converter.

The inductance L_r is the commutation inductor plus the leakage inductances of the transformers Tr_1 and Tr_2 .

The output stage of the proposed converter is formed by the series connection of the secondary center-tapped windings of the transformers Tr_1 and Tr_2 , associated with rectifiers Do_1 and Do_2 and an output filter composed of Lo and Co .

The switches are arranged in two pairs (S_1, S_4 and S_2, S_3). Within each pair, the switches are driven in a complementary way. The total input voltage and the voltage across the multilevel capacitors C_{m1} and C_{m2} impose the voltage across the blocking switch of any pair.

In order to keep the capacitors C_{m1} and C_{m2} voltage stable, the converter has to be modulated in an appropriated manner. The gate signals of the switches are presented in figure 3.

B. Principle of Operation

The following assumptions are made to simplify the analysis:

- the circuit operates in steady-state;
- all components are considered ideal;
- the output filter is large enough to be considered as a current source with a value equal to the load current I_o ;
- the transformers turns ratio is equal to one;

- the inductances L_{m1} and L_{m2} represent the magnetising inductances of the transformers;
- the ripple in the DC voltage across the multilevel capacitors C_{m1} and C_{m2} is negligibly small;
- capacitances C_1 , C_2 , C_3 and C_4 are the MOSFET's intrinsic capacitances incorporating all the transformer's parasitic capacitances;
- there is no difference among the gate signals applied to each pair of switches (S_1, S_4 and S_2, S_3), ie, they have identical duty cycles.

Figure 2 shows the topological stages of the converter for half-period of operation and figure 3 shows the key waveforms for one switching period.

The operation of this converter is similar to the operation of the TL (three-level) DC-DC ZVS PWM converter based on the flying capacitor [4] and can be described as follows.

First Stage (t_0, t_1): Switch S_1 is turned-off at t_0 (the beginning of a switching cycle) and diode D_1 starts to conduct. The load current flows through S_3 , D_1 , C_{m1} and C_{m2} . All output rectifiers are conducting, consequently short-circuiting the output stage. Voltage v_{ac} is zero and voltage v_{bc} is $V_i - V_{C_{m1}}$.

Second Stage (t_1, t_2): When S_3 is turned-off, voltage v_{C3} increases from zero to V_i , while v_{C2} decreases from V_i to zero. This stage ends at t_2 , when D_2 is directed biased and starts conducting. During this stage the current flows through D_1 , C_2 and C_3 . The output stage remains short-circuited. The magnetising currents i_{m1} and i_{m2} flow through capacitors C_{m1} and C_{m2} . Voltage v_{ac} is $V_i - v_{C2}$ and v_{cb} is $V_i - V_{C_{m1}}$.

Third Stage (t_2, t_3): When voltage v_{ac} reaches V_i , the current i_{Lr} starts to increase. While i_{Lr} is negative, flows through diodes D_1 and D_2 . During this period of time S_2 is gated-on at zero-voltage and zero current. When i_{Lr} becomes positive, the current starts to flow through switches S_1 and S_2 . All output rectifiers are conducting and the input voltage is zero. The stage ends when i_{Lr} reaches load current I_o and D_{o2} and D_{o3} start to conduct. The difference between currents i_{m2} and i_{m1} is circulating through capacitor C_{m1} . The current through capacitor C_{m2} is null.

Fourth Stage (t_3, t_4): Power is transferred from the superior source V_i to the load through the switches S_1 and S_2 and diodes D_{o2} and D_{o3} . Magnetising currents i_{m2} and i_{m1} flow through capacitor C_{m1} and current through capacitor C_{m2} remains null.

Fifth Stage (t_4, t_5): This stage begins when S_2 is turned-off. The capacitor C_2 begins to charge and C_3 begins to discharge linearly with time, with a constant current. This stage finishes when v_{C2} reaches V_i , v_{C3} becomes null and D_3 starts to conduct.

The second half period is identical to the first one with switches S_1 and S_4 replacing S_2 and S_3 in the commutation stages.

III. THEORETICAL ANALYSIS

A. Output Characteristics

In the third stage a reduction in the duty ratio occurs because S_2 is gated-on but the free-wheeling in

the output rectifier maintains zero voltage across the load.

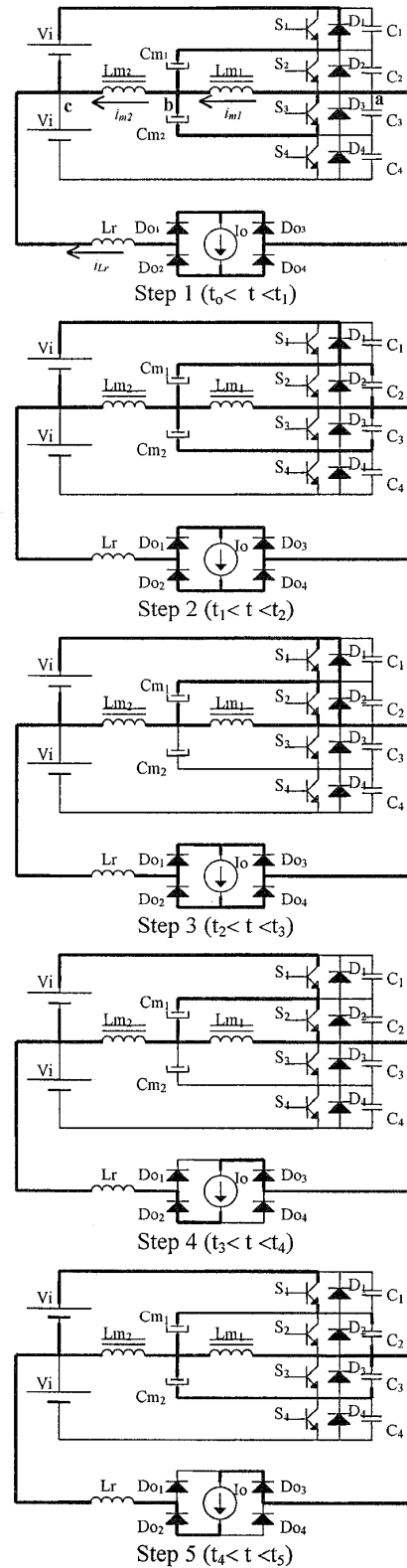


Fig. 2 – Stages of operation.

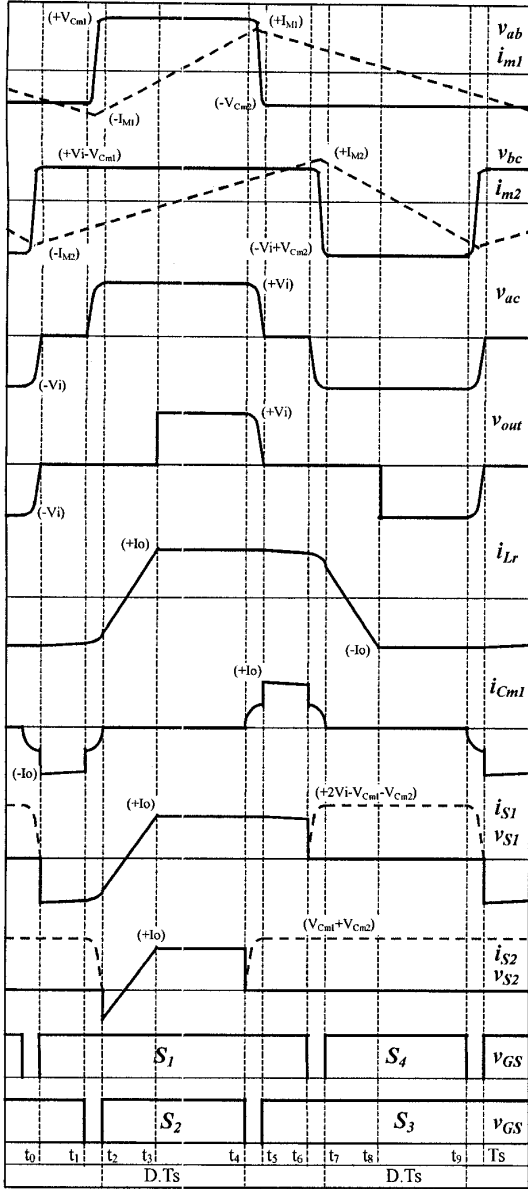


Fig 3 – Key waveforms.

According to the waveforms shown in figure 3, and considering that the commutation time is much smaller than the switching period, the average output voltage is given by

$$V_o = \frac{1}{T_s} \cdot [(D \cdot T_s - \Delta t_3) 2V_i] \quad (1)$$

where:

$2V_i$ - input voltage

D - duty cycle

$\Delta t_3 = t_3 - t_2$

T_s - switching period

Considering the third stage, Δt_3 can be defined as

$$\Delta t_3 = \frac{2 \cdot I_o \cdot L_r}{V_i} \quad (2)$$

Hence

$$q = \frac{V_o}{V_i} = \left(2 \cdot D - 4 \cdot \frac{I_o \cdot L_r \cdot f_s}{V_i} \right) \quad (3)$$

Defining the reduction of the duty-cycle as

$$\Delta = 2 \cdot \frac{I_o \cdot L_r \cdot f_s}{V_i} \quad (4)$$

the effective duty-cycle can be defined as follows:

$$D_{eff} = 2D - 2\Delta \quad (5)$$

The output characteristics shown in figure 4 is similar to those obtained for the converters studied in references [1], [2], [4] and [5].

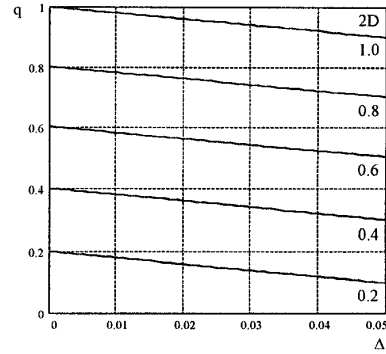


Fig. 4 - Output characteristics of the proposed converter.

From the expression (3), that represents the dc voltage-conversion-ratio of the converter, it can be noticed that the larger L_r is, the larger also is the reduction of the output voltage caused by the reactive voltage drop.

B. Commutation Analysis

This converter presents two different commutation in its switches.

In the first case, on stage 5, the charge/discharge of the capacitors in parallel to the switches occurs with constant current equal to I_o .

The most critical commutation takes place during the second stage where the charge and discharge of the capacitors in parallel with the switches occurs in the resonance stage between the inductor L_r and the capacitors C_2 and C_3 .

The voltage across C_3 during this stage is defined by

$$v_{C3} = \sqrt{\frac{L_r}{2 \cdot C}} \cdot I_o \cdot \sin(\omega_r \cdot t) \quad (6)$$

The current in the inductor L_r is

$$i_{L_r} = -I_o \cdot \cos(\omega_r \cdot t) \quad (7)$$

where:

ω_r - resonant frequency

C - equivalent capacitance in parallel to the switches

Considering expressions (6) and (7), the state plane of this stage can be plotted as shown in figure 5. As can be noticed the following condition must be respected to ensure soft commutation:

$$I_o \geq \sqrt{\frac{2C}{L_r}} \cdot V_i \quad (8)$$

Thus

$$I_{o_{\min}} = \sqrt{\frac{2C}{L_r}} \cdot V_i \quad (9)$$

The wider the load range with ZVS is, which implies smaller minimum load current $I_{o_{\min}}$, the higher is the reactive voltage drop across commutation inductor L_r . A good design involves sacrificing the soft-commutation at light load, where the conduction losses are low, to obtain high efficiency at full-load.

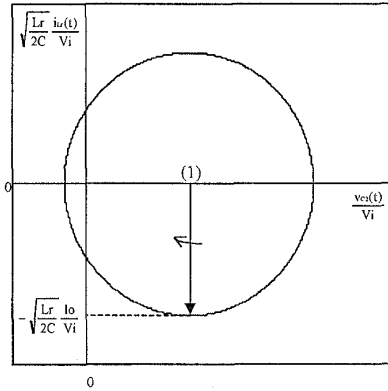


Fig. 5 - State plane of stage 2.

C. Voltage Sharing

The maximum voltage across the pair of switches S_1, S_4 and S_2, S_3 (figure 3) are defined by

$$V_{S14 \max} = 2V_i - (V_{Cm1} + V_{Cm2}) \quad (10)$$

$$V_{S23 \max} = (V_{Cm1} + V_{Cm2}) \quad (11)$$

Considering that, in steady state operation, the average voltage across the magnetising inductance of the transformers is zero, the following equations are obtained:

$$V_{Cm1} = V_i(1 - D) \quad (12)$$

$$V_{Cm2} = V_i D \quad (13)$$

Therefore

$$V_{Cm1} + V_{Cm2} = V_i \quad (14)$$

Consequently the maximum voltage across any blocking switch is half of the input voltage $2V_i$.

IV. SIMPLIFIED DESIGN EXAMPLE

The design procedure of the converter presented in this paper is similar to that of the FB-ZVS-PWM converter [1,6], of the TL-ZVS-PWM converter based on the NPC cell [2] and of the TL-ZVS-PWM converter based on the flying capacitor cell [4].

A simplified approach is presented in this section, using deduced equations to define the components for the implementation of a prototype.

A. Input Data

Rated output power: $P_o = 1.5 \text{ kW}$

Input Voltage: $2V_i = 600 \text{ V}$
 Output voltage: $V_o = 60 \text{ V}$
 Switching frequency: $f_s = 50 \text{ kHz}$
 Output inductor ripple: $\Delta I_o = 2.5 \text{ A}$
 Output voltage ripple: $\Delta V_o = 0.06 \text{ V}$
 Multilevel voltage ripple: $\Delta V_{Cm} = 3 \text{ V}$
 Maximum duty cycle: $2D = 0.8$

B. Passive Components

1) *Transformers Tr_1 and Tr_2* : Considering a maximum nominal duty-cycle reduction (Δ) equal to 15% of the nominal value of D :

$$D_{\text{eff}} = D - 0.15D = 0.34$$

The transformer turns ratio can be calculated from:

$$n = \frac{N_p}{N_s} = n_{Tr1} = n_{Tr2} = \frac{V_i}{V_o} \cdot 2 \cdot D_{\text{eff}} = 3.4$$

2) *Resonant inductor L_d* : Considering the maximum duty-cycle reduction specified, the resonant inductor can be calculated from:

$$L_d = \frac{\alpha \cdot V_i \cdot n}{2 \cdot I_o \cdot f_s} = 24.5 \mu\text{H}$$

3) *Multilevel capacitors C_{m1} and C_{m2}* : The multilevel capacitors must be large enough to be considered as voltage sources. Thus the required value of these capacitors is calculated as a function of the maximum allowable voltage ripple (ΔV_{Cm}) using the following expression:

$$C_m = \frac{I_o \cdot (1 - D)}{2 \cdot n \cdot \Delta V_{Cm} \cdot f_s} = 5 \mu\text{F}$$

4) *Output filter L_o and C_o* : The inductance and capacitance of the output filter are calculated employing the following expressions:

$$L_o = \frac{V_i}{8 \cdot f_s \cdot n \cdot \Delta I_o} = 89 \mu\text{H}$$

$$C_o = \frac{\Delta I_o}{8 \cdot f_s \cdot \Delta V_o} = 10 \mu\text{F}$$

C. Switches Voltage and Current Stresses

1) *Active Switches*: The maximum voltage across the blocking switches is

$$V_{D_{S \max}} = V_i = 300 \text{ V}$$

The rms current through the switches S_1 and S_3 can be calculated by

$$I_{S13 \text{ rms}} = \frac{I_o}{n} \cdot \sqrt{\frac{1 - \alpha}{2} - \frac{\alpha}{3}} \therefore I_{S13 \text{ rms}} = 5.66 \text{ A}$$

Through the switches S_2 and S_4 the rms current is:

$$I_{S24 \text{ rms}} = \frac{I_o}{n} \cdot \sqrt{D - \frac{\alpha}{3}} \therefore I_{S24 \text{ rms}} = 5.03 \text{ A}$$

2) *Output rectifier*: In the output rectifier, the diode reverse voltage is:

$$V_{D_{\max}} = 2 \cdot \frac{V_i}{n} = 176.47 \text{ V}$$

The diode's average current is given by

$$I_{D_{avg}} = \frac{I_o}{2} = 12.5A$$

V. EXPERIMENTAL RESULTS

Based on the design given in section IV a breadboard has been implemented.

The power stage of the converter is shown in figure 6, which consists on the following components

S_{1-4}	IRFP460 - 500V, 20A (Harris)
D_{O1-2}	MUR 1560 - 600V, 15A (Motorola)
Tr_{1-2}	2 ferrite cores E65/26 - IP 12 (Thornton) Primary: 17 turns - Secondary: 10 turns - Center tapped
L_r	15.8 μ H - ferrite core E42/15 - IP 12 (Thornton)
L_o	89 μ H - ferrite core E 55/20 - IP 12 (Thornton)
C_o	220 μ F/100V - electrolytic (Icotron)
C_m	7 μ F/400V - polyester (Icotron)
D_g	MUR 140 (Motorola)
C_g	10nF - polypropylene (Icotron)
R_g	24k Ω , 2W

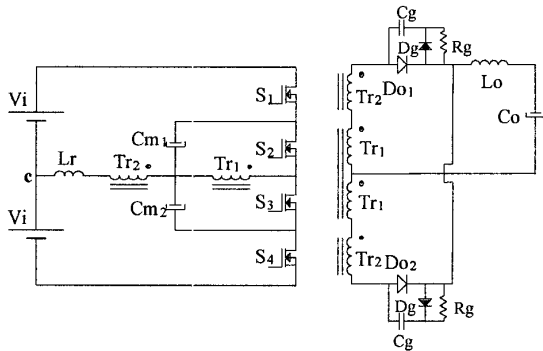


Fig. 6 - Power stage diagram of the implemented converter.

The total resonance inductance is composed by the leakage transformer inductances (4.3 μ H and 4.1 μ H) and the external resonance inductance (15.8 μ H), yielding 24.2 μ H. The MOSFET's body diodes were used for D_{1-4} of figure 1, and the MOSFET's Coss capacitances (480pF) were used for C_{1-4} .

Experimentally obtained waveforms for $P_o = 1.5kW$, $I_o = 25A$, $2V_i = 600V$, $f_s = 50kHz$ and $D = 0.8$ are shown in figures 7, 8, 9 and 10. They confirm the theoretically predicted results.

Figures 8 and 9 demonstrate the principal characteristics of the proposed converter topology: the maximum voltage across the switches is 300V, half of the 600V DC input voltage and the zero-voltage switching.

The output characteristic of the converter for $2V_i = 600V$ and $D = 0.8$ is presented in figure 11, which confirms the expression (3), with the output

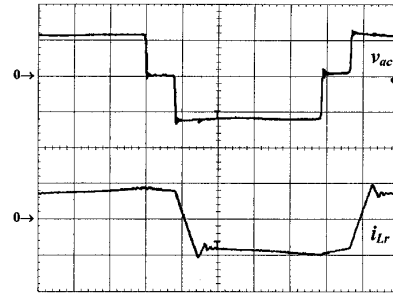


Fig. 7 – Experimental waveforms.
Upper trace: v_{ac} voltage (250V/div. 2 μ s/div.)
Lower trace: i_{Lr} current (10A/div. 2 μ s/div.)

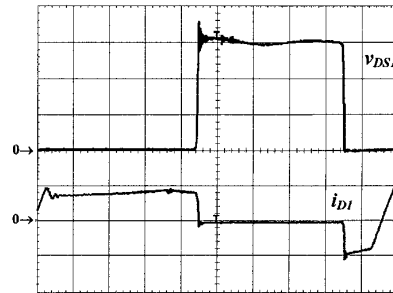


Fig. 8 – Experimental waveforms - switch S_1 .
Upper trace: drain-to-source voltage v_{DS1}
(100V/div. 2 μ s/div.)
Lower trace: drain current i_{D1} (10A/div. 2 μ s/div.)

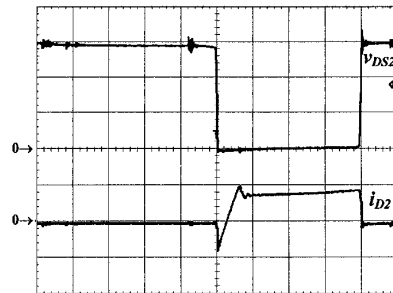


Fig. 9 – Experimental waveforms - switch S_2 .
Upper trace: drain-to-source voltage v_{DS2}
(100V/div. 2 μ s/div.)
Lower trace: drain current i_{D2} (10A/div. 2 μ s/div.)



Fig. 10 – Experimental waveforms - diode D_{O1} .
Upper trace: cathode-anode voltage v_{Do1}
(100V/div. 2 μ s/div.)
Lower trace: anode current i_{Do1} (10A/div. 2 μ s/div.)

voltage decreasing with an increase of the output current due to the reduction of effective duty-cycle, caused by the amount of reactive power that circulates in the circuit.

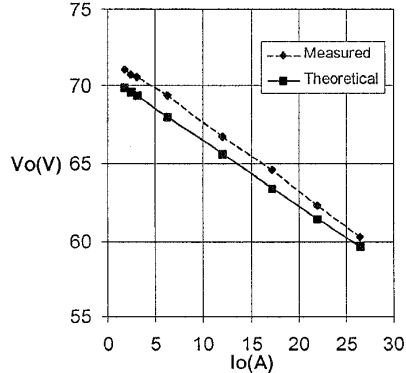


Fig. 11 – Output voltage V_o versus output current I_o .

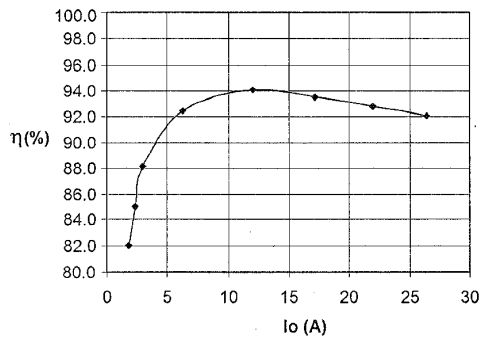


Fig. 12 - Measured efficiency as a function of the load current.

The experimentally measured efficiency as a function of the load current is shown in figure 12, for constant input voltage equal to 600V. The efficiency at full load (25A) is 92%. The maximum efficiency at 12.5A (50%) was 94.1%. The main source of losses are diode and MOSFET conduction losses, magnetic and snubber losses. The switching losses at full load are practically zero.

The theoretical ZVS load range for this converter is 6.42A to 25A. For currents lower than 6.42A the ZVS commutation is lost, and the converter starts to operate with hard-switching. This also can be confirmed by figure 12, where the efficiency clearly decreases for load currents lower than 6A.

VI. CONCLUSIONS

In this paper it was presented the analysis, simplified design procedure and experimental results of a three-level ZVS PWM DC-to-DC converter based on a modified flying capacitor multilevel topology.

The results obtained lead to the following conclusions:

- the proposed converter presents identical characteristics to the three-level DC-to-DC converters based on the NPC inverter [2] and on the flying capacitor cell [4];

- the converter presents high-efficiency (92% at full load) due to ZVS commutation on the switches;
- the output voltage decreases with an increase of the output current due to the reduction of effective duty-cycle caused by the amount of reactive power circulating in the circuit (presence of L_r);
- half of the input voltage across the blocking switches makes this converter suitable for high input voltage applications;
- possibility of sharing the output power between the power transformers makes the proposed converter suitable for high power applications.

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