

A ZVS Clamping Mode – Current-Fed Push-Pull DC-DC Converter

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Abstract - This paper introduces a new technique to recover the energy trapped in the leakage inductor of the current-fed push-pull converter, by means of an active clamping mode circuit. Theoretical analysis and experimental results, taken from a 800W/40KHz are presented in the paper. The studied converter also features ZVS (zero voltage switching) in all switches, preserving all the main properties of the original circuit. As a result, the efficiency is improved and the electromagnetic disturbances are minimized.

With a correct parametric combination, ZVS (zero voltage switching) can be achieved. The active clamping technique was proposed in [2] in a forward converter and generalized in [3].

II. THE PROPOSED CIRCUIT AND PRINCIPLE OF OPERATION

I. INTRODUCTION

The current-fed push-pull converter is illustrated in Fig. 1. This converter was patented in 1976 [1], and features good load regulation. Besides that, it does not present the flux accumulation problem due to the unbalance in the conduction times of the main switches. However, it has an inherent problem due to the energy stored in the leakage inductances of the push-pull transformer. If a path is not provided for this energy, the main switches are penalized with severe voltage overshoots, and the practical implementation of the circuits becomes unfeasible. The two possible techniques to solve such problems are nominated *passive clamping* and *active clamping*. A passive clamping technique is exemplified in Fig. 2.

The passive clamping techniques solve the voltage overshoot problem, however it diminishes the converter's overall efficiency, since the energy is wasted through the clamping resistor R_c .

The active clamping techniques promote the complete devolution of the energy stored in the leakage inductances. Despite the use of a clamping diode and an auxiliary switch for each main switch, the energy loss problem is solved.

A. Proposed Circuit

The current-fed push-pull converter with active clamping is illustrated in Fig. 3. The main components of the converter in Fig. 3 are: two main switches SM1 and SM2; two anti-parallel diodes D1 and D2; two auxiliary clamping switches Sa1 and Sa2; two clamping diodes Da1 and Da2 and a clamping capacitor Cc. Besides, the current feeding is provided by the constant voltage source V_i in series with the input inductor L. The Push-Pull transformer is represented by the primary windings L_{p1} and L_{p2} and the secondary windings L_{s1} and L_{s2} . As usual, the leakage inductances are referred to the primary side by L_{k1} and L_{k2} (which is the main concern of the active clamping concept); n_p and n_s represent the number of turns in each winding. Finally, the output is constituted by the rectifier diodes D3 and D4, the output filter capacitor C_o and the output resistance R_o ; C1, C2, Ca1 and Ca2 being the commutation capacitors of their respective switches.

B. Main Theoretical Waveforms

Fig. 4 illustrates the main theoretical waveforms of the converter, operating in continuous conduction mode. The main switches operate with superimposed drive signals, with constant frequency, as seen in Figs. 4(a) and 4(b). The drive signals of the auxiliary switches are complementary in relation to their respective main switches, as seen in Figs. 4(c) and 4(d). An inverter leg (for instance, the one formed by SM1, DM1, CM1, Sa1, Da1 and Ca1) constitutes a ZVS commutation cell, operating with a constant 180 degree phase-shift in relation to the other. Power transfer control is achieved through a single voltage reference.

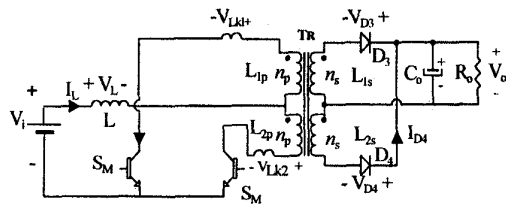


Fig. 1: Current-fed push-pull converter.

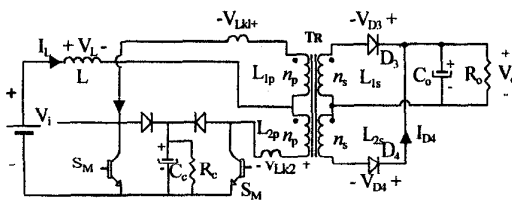


Fig. 2: A passive clamping technique

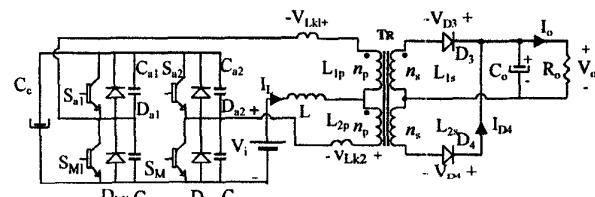


Fig. 3: Proposed circuit

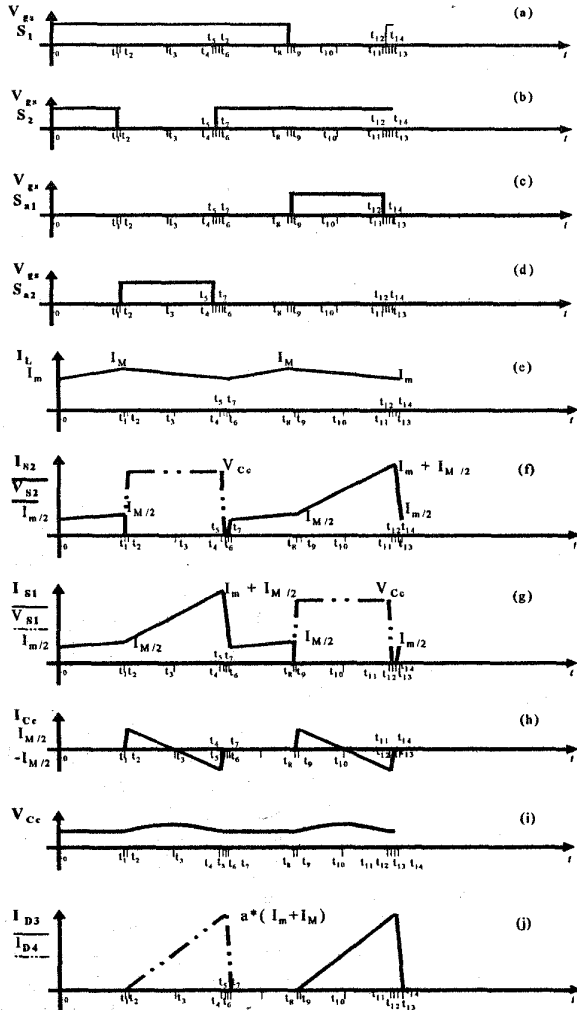


Fig. 4: Main theoretical waveforms.

Fig. 4(e) shows the current through the input inductor, indicating that the circuit behaves, from the standpoint of energy processing, as a boost converter. Figs. 4(g) and 4(f) illustrate the current through, as well as the voltage across, the main switches. The peak current in the switches reaches approximately 1.5 times the input current, being a direct consequence of the active clamping process. Figs. 4(h) and 4(i) illustrate the current flowing through the clamping capacitor and the voltage across its terminals. The current flowing through the auxiliary switches and anti-parallel diodes, reflected in Fig.4(h), features smaller average and peak values. The clamping voltage (Fig. 4(i)), must not present considerable ripple. In Fig. 4(j), “a” represents the primary to secondary turns ratio (np/ns).

C. Stages of Operation

The circuit has seven topologic stages within half of an operation period. The remainder of the operation is analogous to the first semi-period. The seven topologic stages of the converter operation in one semi-cycle are illustrated in Fig. 5. Following is a description of a semi-period, considering steady state operation.

1st Stage ([t₀, t₁] Fig. 5(a)): The current flowing through the primary inductances L_{p1} and L_{p2} have the same

absolute value and opposite direction, causing a magnetic short-circuit in the push-pull transformer. The input inductor L stores energy during this stage. At the end of this stage, the input current reaches its maximum value.

2nd Stage ([t₁, t₂] Fig. 5(b)): At time t₁, the main switch SM2 is turned off. The energy stored in the leakage inductance L_{k2} is redirected to the commutation capacitors C₂ e C_{a2}. The voltage in the main switch SM2 rises smoothly to the value V_{Cc}, which is the constant voltage in the clamping capacitor C_c. From this stage, until the end of the fifth stage, the energy stored in the input inductor is transferred to the load through the main switch S1 and the rectifier diode D4. In this stage, ZVS commutation is accomplished.

3rd Stage ([t₂, t₃] Fig. 5(c)): At instant t₂, the clamping diode Da2 redirects the energy stored in the leakage inductance L_{k2} to the clamping capacitor C_c. The energy exchange between L_{k2} and C_c occurs in resonant fashion. The auxiliary switch Sa2 must be enabled to conduct during this stage.

4th Stage ([t₃, t₄] Fig. 5(d)): At time t₃ the clamping capacitor starts to return the energy received during the 3rd stage, through Sa2, in resonant mode.

5th Stage ([t₄, t₅] Fig. 5(e)): At the instant t₄ the auxiliary switch Sa2 is turned off and the commutation starts. The voltage in the main switch falls smoothly to zero. Notice that the amount of energy available to this commutation is practically the same as in the third stage.

6th Stage ([t₅, t₆] Fig. 5(f)): At time t₅, diode DM2 starts to conduct and the energy of the leakage inductances L_{k1} and L_{k2} is transferred to the load. The voltage in the leakage inductances is such that the input inductor is virtually in parallel to the input voltage source V_i. During this stage the currents in main switch SM1 and in the diode DM2 decrease rapidly. The main switch SM2 must be enabled to conduct during this stage.

7th Stage ([t₆, t₇] Fig. 5(g)): At the instant t₆, the current in diode D2 reaches zero and inverts its direction, flowing through SM2. The current in SM1 maintains its decreasing slope and the current in SM2 increases with an inverted slope.

III. MAIN THEORETICAL RESULTS

The analytical expression for the external characteristic of the converter (in continuous conduction mode only) is presented below:

$$G = \frac{V_{op}}{V_i} = \frac{1}{1-D+2 \cdot I_n} \quad (1)$$

where:

$$I_n = \frac{f \cdot L_d \cdot I_{op}}{V_i} \quad (2)$$

$$I_{op} = \frac{ns}{np} I_o \quad (3)$$

$$V_{op} = \frac{np}{ns} V_o \quad (4)$$

and

$$D = \frac{t_g - t_5}{T/2} = \frac{\Delta t_{g,5}}{T/2} \quad (5)$$

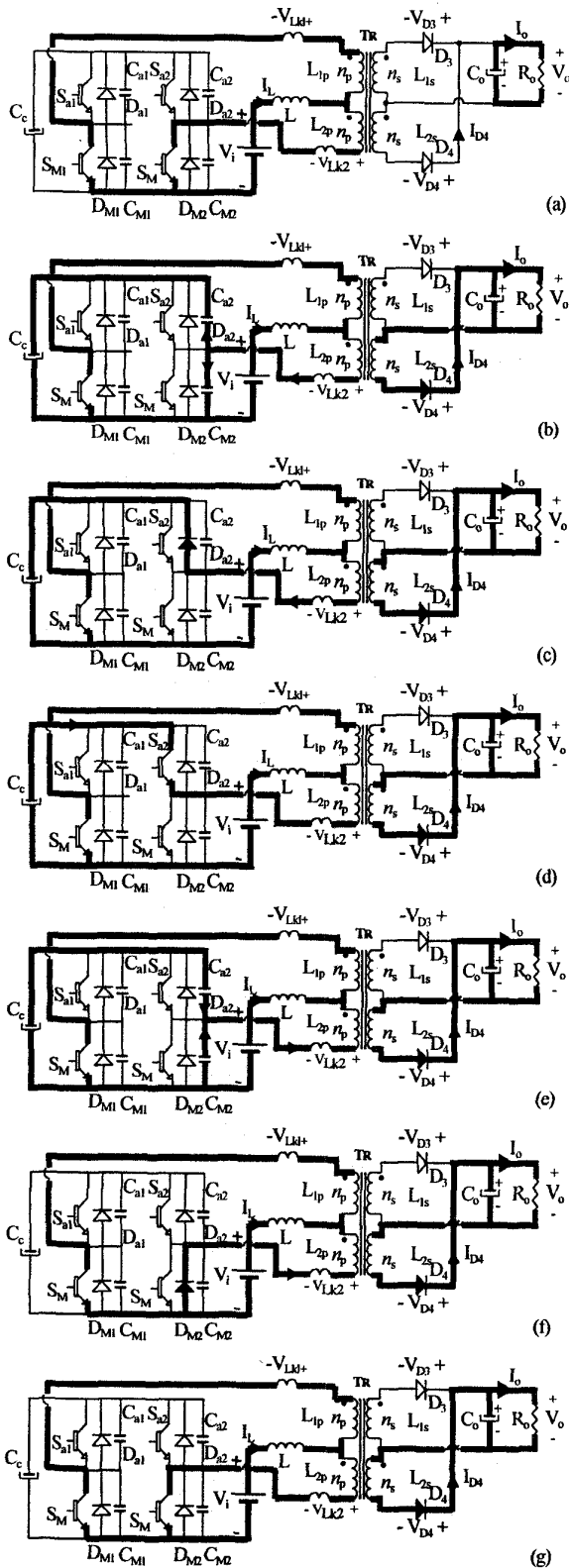


Fig. 5: Topological states of the converter operation

In (1), the converter normalized voltage gain G is presented as a function of the normalized output current I_n , with the converter duty cycle D as a parameter. The converter duty cycle is defined as the normalized time interval, within a semi-period of operation, in which the

conduction of the main switches overlap. Referring to Figs. 4(a) and 4(b), it is mathematically expressed in (5).

I_{op} and V_{op} are respectively the output current and the output voltage referenced to the primary side.

The external characteristics (Fig. 6) present a decaying voltage gain, which is due to the reactive energy circulating in the active clamping circuit. The relationship between the converter duty cycle and the output gain is typical of circuits operating with the boost principle.

It has been analytically determined that, disregarding the influence of the input current ripple and the conduction losses, the clamping voltage is independent of the load. Therefore, the clamping voltage can be determined by (6):

$$V_{Cc} = \frac{2 * V_i}{1 - D} \quad (6)$$

Guaranteeing a small input current ripple is a valid design directive, since it is desirable to obtain a small dependence of the clamping voltage on the load.

IV. EXPERIMENTAL RESULTS

Fig. 7 illustrates a prototype assembled in laboratory, which confirmed the analytical and simulation results, as well as the design procedure. The output stage presented in Fig. 8 has been adapted to serve as an input stage for an inverter, maintaining the properties of the converter presented in Fig. 3. The prototype has the following design specifications.

TABLE 1: PROTOTYPE SPECIFICATIONS

Output Power	800 Watts
Output Voltages	250 Volts
Input Voltage	48 Volts

The converter parameters are specified in Table 2:

TABLE 2: PROTOTYPE PARAMETERS

L	144 μ H
$CM1=CM2=Ca1=Ca2$	4.7nF
$a=np/ns$	0.25
Cc	8.4 μ F
$La1=La2$	6 μ H
$Lk1=Lk2$	2 μ H
$Co1=Co2$	150 μ F

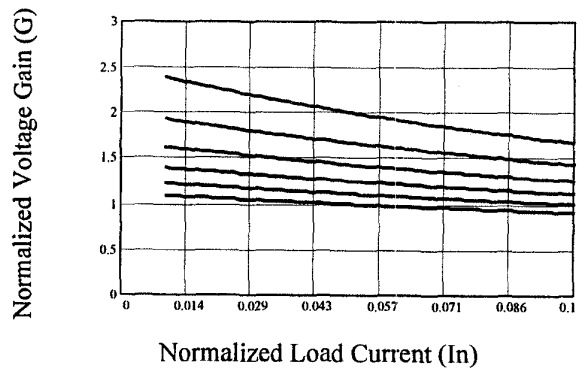


Fig. 6: External Characteristic

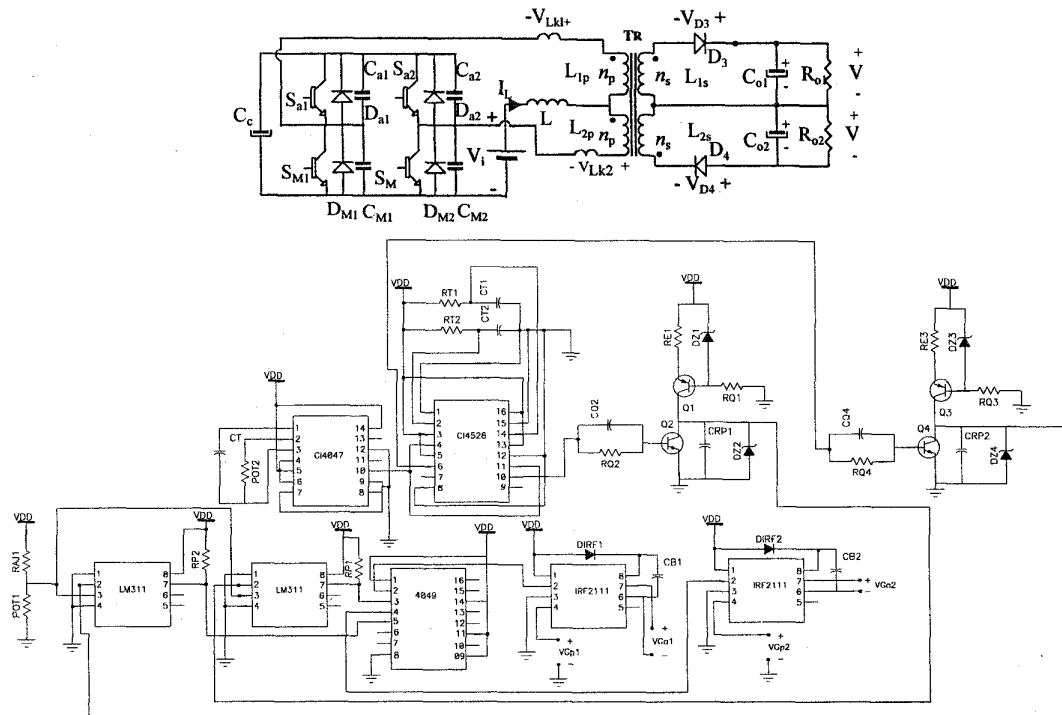


Fig. 7: Complete circuit schematic.

La1 and La2 are auxiliary commutation inductors. Referring to Fig. 3, La1 and La2 are placed in series with Lk1 and Lk2 respectively. The commutation inductors are necessary to guarantee ZVS commutation in a specified load range, namely 40 to 100%.

The switches used are presented in Table 3:

TABLE 3: SEMICONDUCTORS USED IN THE PROTOTYPE

Switches	IRG4PC50U
Anti-parallel Diodes	MUR1520
Rectifier Diodes	MUR860

TABLE 4: INTEGRATED CIRCUITS DESCRIPTION

IC 4047	Astable (D=50%)
CI4528	Dual Monoastable
LM311	Comparator
CI4049	Hex Inverter
IR2111	Isolated Gate Driver

Fig. 8 illustrates the logic used for the generation of the gating signals for the main switches [2]. An astable multivibrator with 50% duty cycle generates the signal in Fig 9(a). With this signal in the input, the dual monoastable multivibrator (see Table 4) generates two outputs (Figs. 9(b),9(c)), which reset the independent voltage ramps seen in Figs. 9(d),9(e). The voltage ramps are compared with one voltage reference, assuring a solid control of the pulse width of both signals.

Fig. 9 illustrates the voltage across and the sum of the currents through SM1, DM1 and CM1. Soft commutation is achieved clearly and the voltage is clamped effectively. It shows also an unbalance between the leakage inductances in the push-pull transformer.

Fig. 10 illustrates the voltage across and the current through Sa1, Da1 and Ca1. The current waveform reflects clearly the energy exchange between the leakage inductances and the clamping capacitor. The exchange is practically linear, since the converter is operating at full load. Fig. 11 illustrates the current through the auxiliary inductors. There is clearly a high frequency exchange, probably between the leakage inductances and the winding capacitances.

Fig. 12 presents a detail of the deadtime needed in order to achieve soft commutation. The gate driver IR2111 is used for this purpose.

Fig. 13 presents the input current. The ripple current is small, but is enough to show the converter duty cycle and the reason for the use of this nomenclature. Noticeable also is that the ripple is at 80KHz.

Fig.14 illustrates the effect of the exchange described above in the push-pull transformer

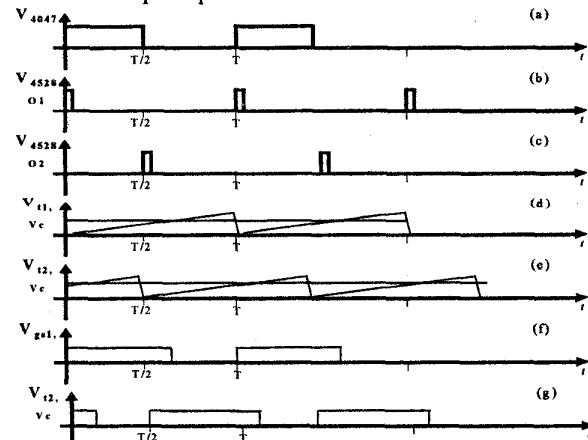


Fig. 8: Gate signal generation for main switches.

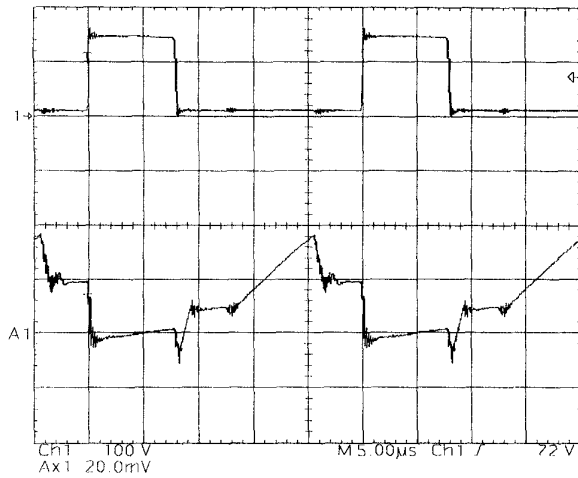


Fig. 9: Voltage across SM1 and current sum through SM1, DM1 and CM1.

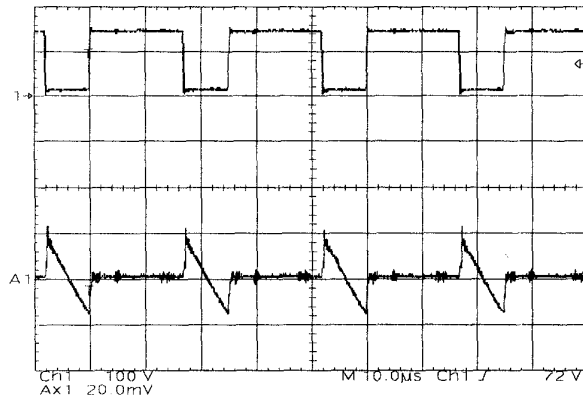


Fig. 10: Voltage across SM1 and current sum through Sa1, Da1 and Ca1.

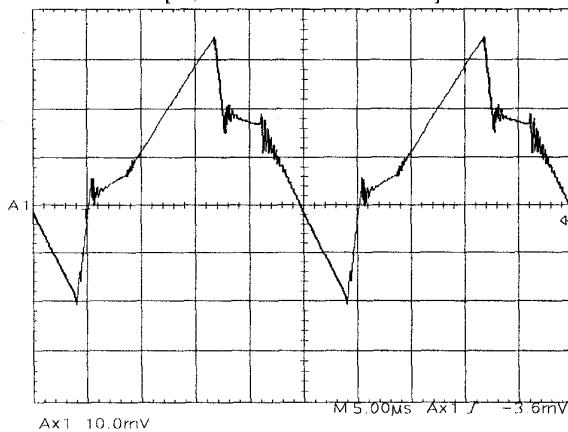


Fig. 11: Current through the commutation inductor.

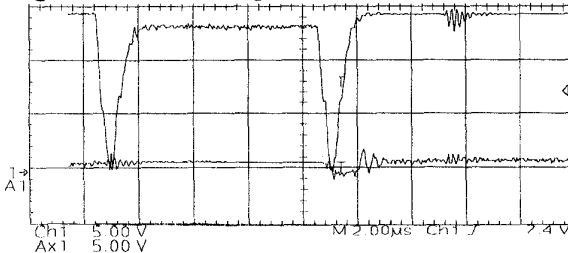


Fig. 12: Complementary gate signals on an inverter leg.

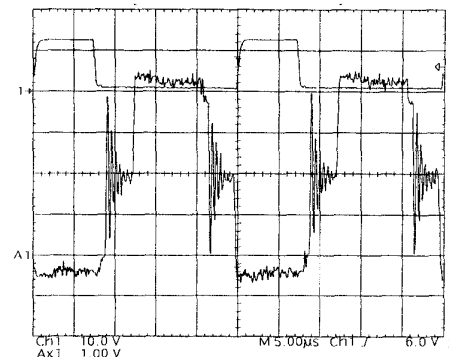


Fig. 13: Voltages in a main switch and in a primary winding

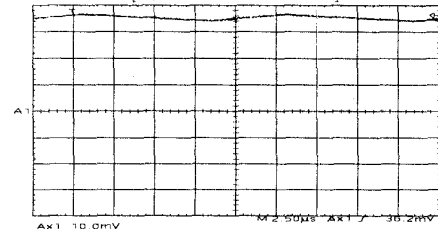


Fig. 14: Current through the input inductor.

V. CONCLUSION

A successful application of the active clamping principle to the current-fed push-pull converter has been achieved through simulation and experimentation.

The principle of operation and the design procedure have been confirmed by simulation and by experimentation. The ZVS (Zero Voltage Switching) property of this converter allowed the increasing of frequency operation, reducing the converters volume and cost, and improving its overall efficiency. Furthermore, as a result of the ZVS technique, the circuit features reduced electromagnetic interference levels.

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