

AN ISOLATED ZVS-PWM DC-TO-DC CONVERTER WITH HALF OF THE INPUT VOLTAGE ACROSS THE SWITCHES

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Abstract – This paper introduces an isolated DC-to-DC converter which features half of the input voltage across the switches, zero-voltage-switching, operation at constant frequency and regulation by pulse-width-modulation. The converter is an alternative for the Full-Bridge ZVS-PWM DC-to-DC converter in high voltage and high power applications. The complete operating principle, theoretical analysis, relevant equations and design example are provided in this paper. The experimental results of a 1.5kW converter with 60V, 25A output, 600V input, operating at 50kHz switching frequency are presented and discussed.

I. INTRODUCTION

In the design of high frequency switching mode power supplies for high power applications, the conventional Full-Bridge Zero-Voltage-Switching Pulse-Width-Modulation (FB-ZVS-PWM) converter [1,2] is considered one of the best alternatives. This converter possesses the most desirable characteristics of both the hard switching PWM and the soft switching converters, while avoiding their major drawbacks, such as commutation losses in the first group, and variable switching frequency and high conduction losses in the second group. However, the conventional FB-ZVS-PWM converter is not suitable for high input voltage applications because the total input voltage is applied across its blocking switches.

Efforts have been made to find alternatives for the conventional FB-ZVS-PWM converter with the purpose of reducing the voltage across the switches allowing the use of popular and low cost semiconductors devices with low blocking voltage capability.

Among the alternatives that have been studied are the multilevel topologies [3,4,5,6,7] that consist of a commutation cell using series-connected semiconductors with clamping circuits ensuring the voltage sharing across the blocking switches. The multilevel technique solves the problems of static and dynamic sharing of the voltage and limits the dv/dt to standard levels.

This paper presents the analysis, design procedure and experimental results of an isolated DC-to-DC converter based on the multilevel technique shown in Fig. 1. This converter is controlled by pulse-width-modulation featuring ZVS commutation and half of the input voltage as the maximum

voltage applied across the switches.

II. CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

A. Circuit Description

The proposed converter is a series association of the primary side of two isolated half-bridge inverters with the secondary of their transformers connected in series. The input voltage (V_i) and the voltage across the capacitors C_{11} to C_{14} impose the voltage across the blocking switches.

The inductances L_{r1} and L_{r2} along with snubbers capacitors C_1 to C_4 provide a resonant transition permitting zero-voltage turn-on eliminating turn-on switching power losses. Capacitors C_1 to C_4 also provide capacitive turn-off snubbing reducing the commutation losses.

The input capacitors C_{11} , C_{12} , C_{13} and C_{14} , along with an appropriate gate signals sequence, are responsible for the voltage clamping across the switches.

The output stage of the converter is formed by the series connection of the secondary center-tapped windings of the transformers T_{r1} and T_{r2} , associated with rectifiers D_{o1} and D_{o2} and an output filter composed of L_o and C_o .

B. Principle of Operation

The following assumptions are made to simplify the analysis:

- all components are considered ideal;
- the output filter is large enough to be considered as a current source with a value equal to the load current I_o ;
- the transformers turns ratio is equal to one;
- the inductances L_{r1} and L_{r2} are referred to the secondary, where:

$$L_{rs} = L_{rs1} = L_{rs2} = 2.(L_{r1} + L_{r2}) \quad (1)$$

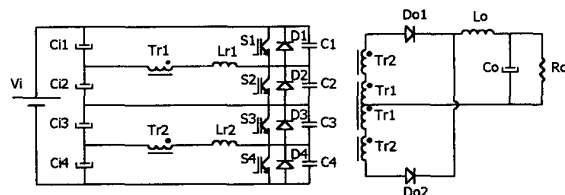


Fig. 1 – The proposed ZVS-PWM DC-to-DC converter.

- the pair of switches (S_1, S_2 and S_3, S_4) have identical duty cycles.

Fig. 2 shows the topological stages of the converter for half-period of operation and Fig. 3 shows the key waveforms for one switching period.

The operation of the proposed converter can be described as follows.

First Stage (t_0, t_1): Switch S_2 is turned-off at the end of the previous cycle and, after the voltage across C_1 had become zero, diode D_1 starts to conduct. The load current flows through S_4, D_1, C_{i1} and C_{i4} . The sum of the transformers voltages is zero. All output rectifiers are conducting, consequently short-circuiting the output stage.

Second Stage (t_1, t_2): When S_4 is turned-off, voltage v_{C4} increases from zero to V_i , while v_{C3} decreases from V_i to zero. This stage ends at t_2 , when D_2 is directed biased and starts conducting. During this stage the current flows through D_1, C_2 and C_3 . The output stage remains short-circuited.

Third Stage (t_2, t_3): When the voltage across the capacitor C_3 becomes null, diode D_2 starts to conduct and the primary current of the transformers T_{r1} and T_{r2} decrease linearly up to zero. During this stage S_2 must be gated-on to achieve zero-voltage switching.

Fourth Stage (t_3, t_4): When the current in the primary of the transformers becomes positive, the current starts to flow through switches S_1 and S_2 . All output rectifiers are conducting and the output voltage is zero. This stage ends when the current of the transformers reaches load current I_o and D_{o2} stops to conduct.

Fifth Stage (t_4, t_5): Power is transferred to the load through the switches S_1 and S_3 and diode D_{o1} .

Sixth Stage ($t_5, T/2$): This stage begins when S_3 is turned-off. The capacitor C_3 begins to charge and C_2 begins to discharge linearly with time, with a constant current. This stage finishes when v_{C3} reaches V_i , v_{C2} becomes null and D_3 starts to conduct.

The second half period is identical to the first one with switches S_1 and S_3 replacing S_2 and S_4 in the commutation stages.

III. THEORETICAL ANALYSIS

A. Output Characteristics

The linear variation of the transformers current during the third and fourth stages causes a reduction in the effective duty-cycle on the load, as shows Fig. 3. This behaviour is given by (2).

$$\frac{V_o}{V_i} = D - \frac{2 \cdot f_s \cdot L_{rs} \cdot I_o}{V_i} \quad (2)$$

where f_s is the switching frequency and D is the duty-cycle.

From (1) that represents the DC voltage conversion ratio of the converter, it can be notice that the larger L_{rs} is, the larger the reduction of the output voltage caused by the reactive voltage drop.

The output characteristics, shown in Fig. 10, are similar to

those of the FB-ZVS-PWM DC-to-DC converter [2].

B. Commutation Analysis

This converter presents two different commutation in its switches.

On the sixth stage, the charge/discharge of the capacitors in parallel to the switches occurs with constant current I_o .

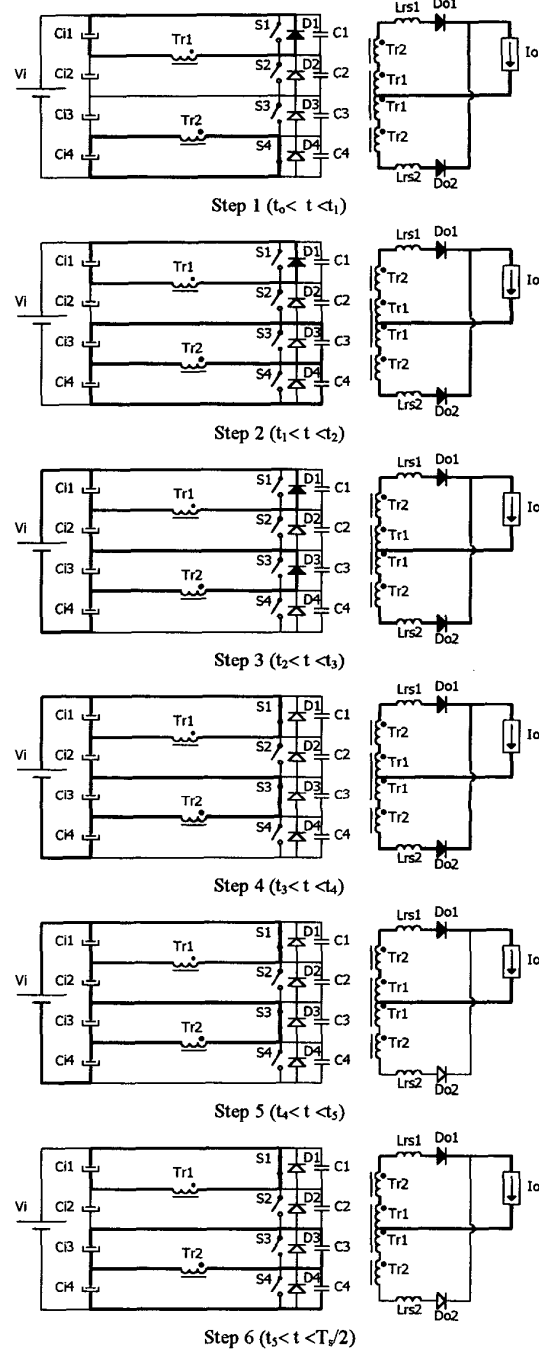


Fig. 2 – Stages of operation.

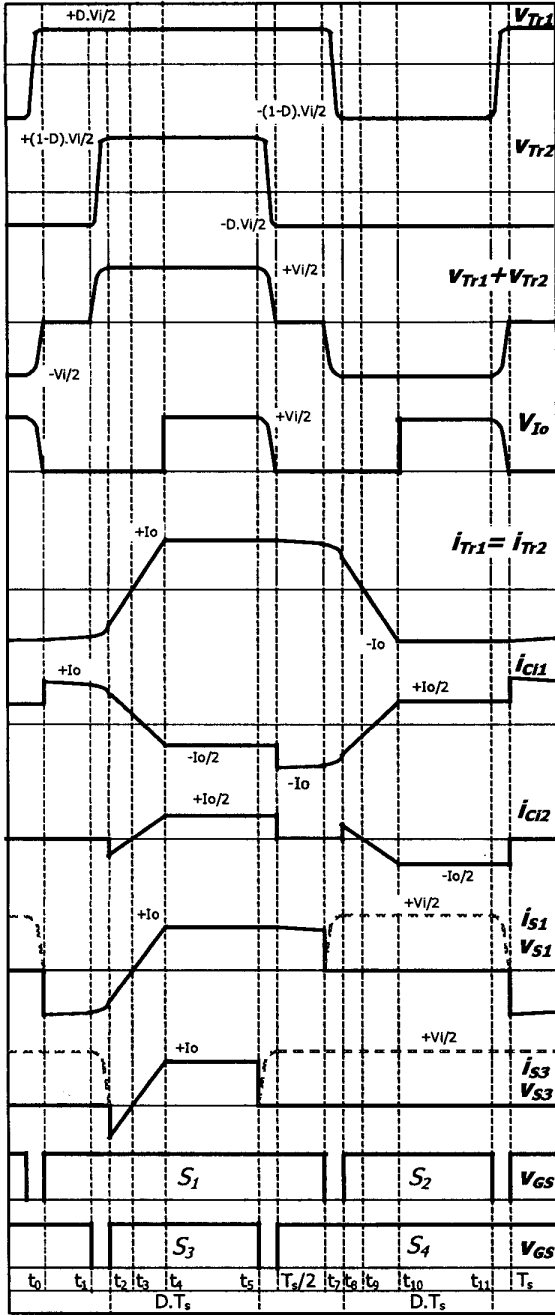


Fig. 3 – Key waveforms.

The most critical commutation takes place during the second stage when the charge and discharge of the capacitors occurs in the resonance stage between the inductors L_{r1} and L_{r2} , and the capacitors C_3 and C_4 . The state plane of this stage is shown in Fig. 4.

From Fig. 4, the following condition must be respected to ensure soft commutation:

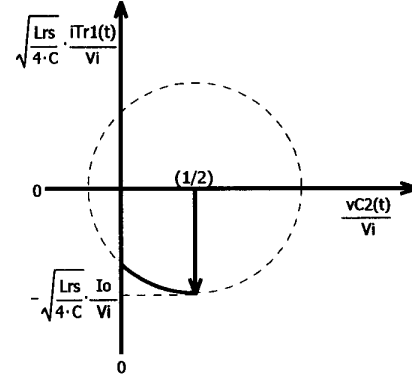


Fig. 4 - State plane of stage 2.

$$\sqrt{\frac{L_{rs}}{4C}} \cdot I_o \geq \frac{V_i}{2} \quad (3)$$

The wider the load range with ZVS is, the higher the reactive voltage drop across L_{r1} and L_{r2} . A good design involves sacrificing the soft commutation at light load, where the conduction losses are low, to obtain high efficiency at full-load.

C. Voltage Sharing

The average value of the voltage across the switches are defined by (4) to (7).

$$V_{S1avg} = (V_{Ci1} + V_{Ci2})D \quad (4)$$

$$V_{S2avg} = (V_{Ci1} + V_{Ci2})(1-D) \quad (5)$$

$$V_{S3avg} = (V_{Ci3} + V_{Ci4})(1-D) \quad (6)$$

$$V_{S4avg} = (V_{Ci3} + V_{Ci4})D \quad (7)$$

Considering:

$$V_{Tr1avg} = V_{Tr2avg} = 0 \quad (8)$$

$$V_{Ci1} + V_{Ci2} = V_{Ci3} + V_{Ci4} = V_i / 2 \quad (9)$$

The voltage across the input capacitors are:

$$V_{Ci1} = V_{Ci4} = \frac{V_i}{2} \cdot D \quad (10)$$

$$V_{Ci2} = V_{Ci3} = \frac{V_i}{2} \cdot (1-D) \quad (11)$$

Thus, the maximum voltage across any switch is half of the input voltage V_i .

IV. SIMPLIFIED DESIGN EXAMPLE

The design procedure of the converter presented in this paper is similar to that of the FB-ZVS-PWM converter [1,2], and of the others ZVS-PWM DC-to-DC converters based on multilevel techniques [4,5,6,7].

A simplified approach is presented in this section, using deduced equations to define the components for the implementation of a prototype.

A. Input Data

Rated output power:	$P_o = 1.5\text{kW}$
Input Voltage:	$V_i = 600\text{V}$
Output voltage:	$V_o = 60\text{V}$
Switching frequency:	$f_s = 50\text{kHz}$
Output inductor ripple:	$\Delta I_o = 2.5\text{A}$
Output voltage ripple:	$\Delta V_o = 0.06\text{V}$
Input voltage ripple (C_{i1-4}):	$\Delta V_{C_{i1-4}} = 6\text{V}$
Input voltage ripple (C_{i2-3}):	$\Delta V_{C_{i2-3}} = 9\text{V}$
Maximum duty cycle:	$D = 0.4$
Maximum duty-cycle reduction:	15%
ZVS load range:	30-100%

B. Passive Components

1) *Transformers turns ratio*: The reduction of the duty-cycle can be calculated by (12), and the transformers turns-ratio by (13).

$$\Delta D = 0.15 D_{max} = 0.06 \quad (12)$$

$$n = \frac{V_i}{V_o} \cdot (D_{max} - \Delta D) = 3.4 \quad (13)$$

2) *Resonant inductances*: The resonant inductance, taking into consideration the duty-cycle reduction, is calculated by (14).

$$L_{tot} = \frac{\Delta D \cdot V_i \cdot n}{4 \cdot I_o \cdot f_s} = 24.5 \mu\text{H} \quad (14)$$

Subtracting the total leakage inductance of the transformers ($8.4\mu\text{H}$), one obtains L_{r1} and L_{r2} equal to $8\mu\text{H}$.

3) *Input capacitances*: The input capacitances to meet the input ripple requirements can be calculated by (15) and (16).

$$C_{i1} = C_{i4} = \frac{I_o}{2 \cdot n \cdot f_s \cdot \Delta V_{C_{i1-4}}} \cdot \left(\frac{1}{2} - D_{max} \right) = 7 \mu\text{F} \quad (15)$$

$$C_{i2} = C_{i3} = \frac{I_o \cdot D_{max}}{2 \cdot n \cdot f_s \cdot \Delta V_{C_{i2-3}}} = 3 \mu\text{F} \quad (16)$$

4) *Output filter*: The inductance and capacitance of the output filter are calculated using (17) and (18).

$$L_o = \frac{V_i}{16 \cdot n \cdot \Delta I_o \cdot f_s} = 89 \mu\text{H} \quad (17)$$

$$C_o = \frac{I_o}{8 \cdot f_s \cdot \Delta V_o} = 10 \mu\text{F} \quad (18)$$

C. Switches Voltage and Current Stresses

1) *Active Switches*: The Mosfet selection to perform ZVS at high frequency must be done considering the rated rms

drain current, peak current and maximum drain-to-source voltage that can be calculated using (19), (20) and (21).

$$I_{Drms} = \frac{I_o}{n} \sqrt{\frac{1}{2} - \frac{5}{6} \Delta D} \therefore I_{Drms} = 4.93\text{A} \quad (19)$$

$$I_{Dpk} = \frac{I_o}{n} \therefore I_{Dpk} = 7.35\text{A} \quad (20)$$

$$V_{DSmax} = \frac{V_i}{2} \therefore V_{DSmax} = 300\text{V} \quad (21)$$

The IRFP460 MOSFET was chosen as it meets the above mentioned requirements.

2) *Output rectifier*: The diodes must be selected taking into consideration the rated average current, peak current and maximum reverse voltage that can be calculated using (22), (23) and (24).

$$I_{Doavg} = \frac{I_o}{2} \therefore I_{Doavg} = 12.5\text{A} \quad (22)$$

$$I_{Dopk} = I_o + \frac{\Delta I_o}{2} \therefore I_{Dopk} = 26.25\text{A} \quad (23)$$

$$V_{DRM} = \frac{V_i}{n} \therefore V_{DRM} = 176.47\text{V} \quad (24)$$

The MUR 1560 diode was chosen as it meets these requirements.

3) *Output rectifier diodes clamping circuits*: To reduce the switching losses on the rectifier diodes, ultra-fast diodes were selected. The interaction of the reverse-recovery process of the rectifier with the leakage inductances of the transformers causes voltage overshoot and ringing.

A voltage clamp circuit can be used to limit the maximum voltage across the diodes [8]. This circuit can be selected as follows.

Considering a clamping voltage V_{cp} equals 211V, the power that will be dissipated in the clamping circuit can be determined by (25).

$$P_{cp} = \frac{1}{2} \cdot f_s \cdot C_{gd} \cdot V_{DRM}^2 \cdot \left[\frac{(1+\mu)^2 \cdot (1-\mu)}{\mu} \right] = 2.01\text{W} \quad (25)$$

where:

$$\mu = \frac{V_{cp} - V_{DRM}}{V_{cp}} \quad (26)$$

The resistance and capacitance of the clamping circuit can be calculated by (27) and (28).

$$R_g = \frac{V_{cp}^2}{P_{cp}} \therefore R_g = 22\text{k}\Omega \quad (27)$$

$$C_g = \frac{1}{0.1 R_g \cdot f_s} \therefore C_g = 10\text{nF} \quad (28)$$

D. ZVS Load Range

The minimum output current that guarantees zero-voltage-switching can be determined by (29).

$$I_{O \min} = n \cdot \frac{V_i}{2} \cdot \sqrt{\frac{2C_{ds}}{L_{rtot}}} = 5.8 \text{ A} \quad (29)$$

where C_{ds} is the drain-to-source capacitance of the Mosfet.

This ensures a ZVS load range of 23.2% to 100%, which meets the soft switching requirements.

V. EXPERIMENTAL RESULTS

Based on the design given in section IV a prototype has been implemented. The power stage of the converter is shown in Fig. 5, consisting on the following components:

S_{1-4}	IRFP460 - 500V, 20A (Harris)
D_{o1-2}	MUR 1560 - 600V, 15A (Motorola)
T_{r1-2}	Ferrite core E65/39 - IP 12 (Thornton) Primary: 17 turns - Secondary: 5+5 turns
L_{r1-2}	8 μ H - ferrite core E30/7 - IP 12 (Thornton)
L_o	89 μ H - ferrite core E 55/28/21 - IP 12 (Thornton)
C_o	220 μ F/100V - electrolytic (Icotron)
$C_{i1-2-3-4}$	7x1 μ F/200V - polyester (Icotron)
D_g	MUR 140 (Motorola)
C_g	10nF - polypropylene (Icotron)
R_g	24k Ω , 2W

The Mosfet's body diodes were used for D_1 to D_4 and the Mosfet's intrinsic capacitances for C_1 to C_4 of Fig. 1.

Experimentally obtained waveforms for P_o equal to 1.5kW, I_o of 25A, V_i equal to 600V, f_s of 50kHz and D equal to 0.42 are shown in Fig. 6, 7, 8 and 9. They confirm the theoretically predicted results.

Fig. 7 and 8 confirm the main characteristics of the proposed converter topology: the maximum voltage across the switches is 300V, half of the 600V DC input voltage and the zero-voltage switching.

The theoretical and output characteristics of the converter for different values of D are presented in Fig. 10, which confirms (2) with the output voltage decreasing with an increase of the output current due to the reduction of the effective duty-cycle.

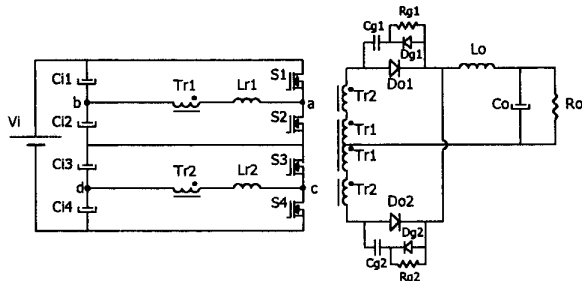


Fig. 5 - Power stage diagram of the implemented converter.

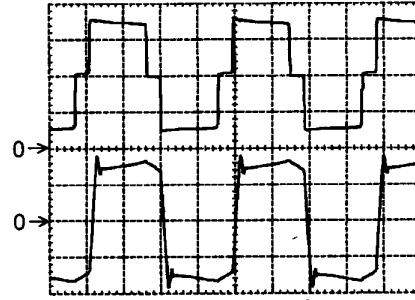


Fig. 6 - Experimental waveforms.

Upper trace: $v_{ab} + v_{cd}$ voltage (250V/div. 5 μ s/div.)
Lower trace: i_{Lr1} current (5A/div. 5 μ s/div.)

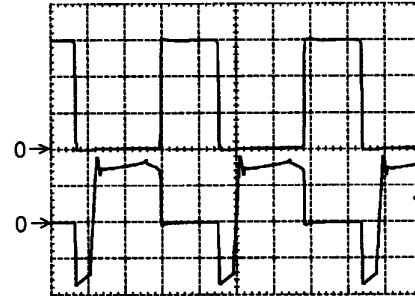


Fig. 7 - Experimental waveforms - switch S_1 .

Upper trace: drain-to-source voltage v_{S1}
(100V/div. 5 μ s/div.)
Lower trace: drain current i_{D1} (10A/div. 5 μ s/div.)

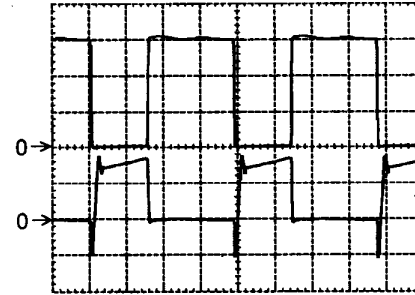


Fig. 8 - Experimental waveforms - switch S_2 .

Upper trace: drain-to-source voltage v_{S2}
(100V/div. 5 μ s/div.)
Lower trace: drain current i_{D2} (10A/div. 5 μ s/div.)

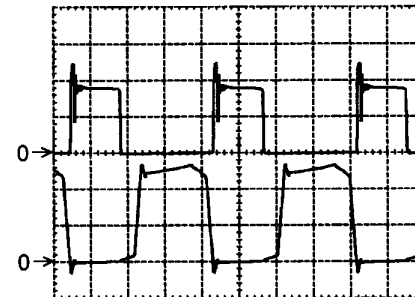


Fig. 9 - Experimental waveforms - diode D_{o1} .

Upper trace: cathode-anode voltage $v_{D_{o1}}$
(100V/div. 5 μ s/div.)
Lower trace: anode current $i_{D_{o1}}$ (10A/div. 5 μ s/div.)

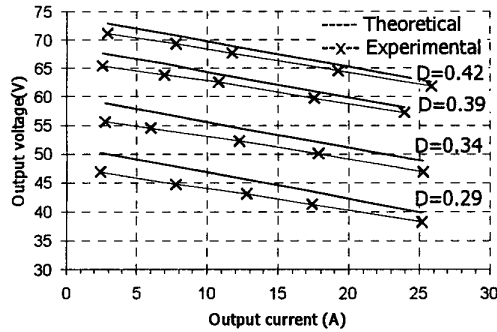


Fig. 10 – Output voltage as a function of output current.

The experimentally measured efficiency as a function of the load current, with constant output voltage and equal to 60V, is shown in Fig. 11. The efficiency at full load (25A) is equal to 92.5%. The maximum efficiency at 10.4A was 94.7%.

The main sources of losses are Mosfet and diode's conduction losses, magnetic and snubber losses. The power losses distribution of the converter, in p.u., is presented in Fig. 12.

The theoretical ZVS load range for this converter is 5.8A to 25A. For currents lower than 5.8A the ZVS commutation is lost, and the converter starts to operate with hard-switching. This also can be confirmed by Fig. 11, where the efficiency clearly decreases for load currents lower than 6A.

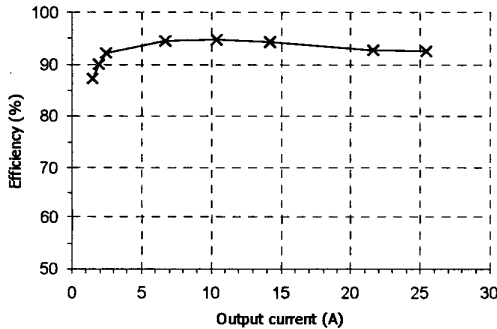


Fig. 11 - Measured efficiency as a function of the load current.

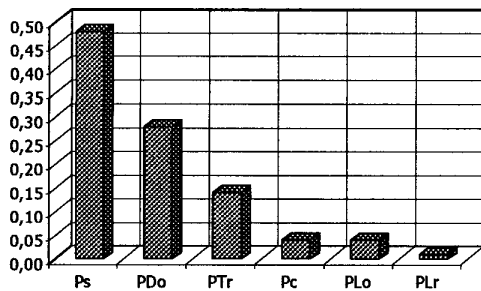


Fig. 12 – Theoretical power losses distribution of the converter in p.u.

VI. CONCLUSIONS

The analysis, simplified design procedure and experimental results of an isolated ZVS-PWM DC-to-DC converter based on the series association of half-bridge converters was presented in this paper.

The results obtained with the proposed converter lead to the following conclusions:

- the proposed converter presents identical characteristics to the FB-ZVS-PWM DC-to-DC converter [1,2] and to other isolated ZVS-PWM DC-to-DC converters based on multilevel techniques [4,5,6,7];
- high-efficiency (92.5% at full load) due to ZVS commutation on the switches;
- half of the input voltage across the blocking switches makes this converter suitable for high input voltage applications;
- possibility of sharing the output power between the power transformers makes the proposed converter suitable for high power applications;
- the reduction of the voltage levels across the switches reduces the dV/dt and the EMI to standard levels;

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REFERENCES

- [1] R.A. Fisher, K.D.T. Ngo and M.H. Kuo, "500 kHz 250 W DC-DC Converter with Multiple Output Controlled by Phase-Shift PWM and Magnetic Amplifiers", *High Frequency Power Conversion 1988 Conference Records*, pp.100-110.
- [2] J.A. Sabaté, V. Vlatkovic, R.B. Ridley, F.C. Lee and B.H. Cho, "Design considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter", *APEC'90 Conference Records*, pp. 275-284.
- [3] T.A. Meynard and H. Foch, "Multilevel Conversion: High-Voltage Choppers and Voltage-Source Inverters", *PESC'92 Conference Records*, pp. 397-403.
- [4] J. R. Pinheiro and I. Barbi, "The Three-Level ZVS PWM DC-to-DC Converter", *IEEE Trans. on Power Electronics*, vol. 8, no. 4, pp. 486-492, October 1993.
- [5] R. Gules, I. Barbi, N.O. Sokal and R. Redl, "DC/DC Converter for High Input Voltage: Four Switches with Peak Voltage of $V_{in}/2$, Capacitive Turn-off Snubbing and Zero-Voltage Turn-on", *PESC'98 Conference Records*, pp. 1-7.
- [6] E. Deschamps and I. Barbi, "A Three-Level ZVS PWM DC-to-DC Converter Using the Versatile Multilevel Commutation Cell", *COBEP'97 Brazilian Power Electronics Conference Records*, pp. 85-90.
- [7] E. Deschamps and I. Barbi, "A New DC-to-DC ZVS PWM Converter for High Input Voltage Applications", *PESC'98 Conference Records*, pp. 967-972.
- [8] L.H. Mweene, C.A. Wright and M.F. Schlecht, "A 1kW 500kHz Front-End Converter for a Distributed Power Supply System", *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 398-407, July 1991.