

# Three-Phase Rectifier Using a Sepic DC-DC Converter in Continuous Conduction Mode for Power Factor Correction

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**Abstract** - This paper presents an analysis of a three-phase rectifier with high power factor using a Sepic DC-DC converter operating in continuous conduction mode (CCM). The structure is particularly simple and robust. Its main features are: one power processing stage, which can operate as step-down or step-up voltage, lower harmonic distortion in the line current and natural isolation. The converter works with constant frequency and PWM modulation. A study for steady state conditions and a design procedure are presented, and experimental results obtained from a laboratory prototype are also presented.

## I. INTRODUCTION

Three-phase feeding systems, available in industrial applications, are usually indicated for high-power systems (over 1kW), where AC/DC conversion has been dominated by conventional diode rectifiers and thyristor controlled rectifiers. The non-linear characteristic of the input current of these rectifiers creates problems for the commercial electric power network, among which the following can be pointed out: increased losses in the distribution and transmission lines of the power network, reduction of power factor, need for generating large quantities of reactive power, electromagnetic interference in control and communication system, distortion of the input voltage, and the decrease in efficiency of structure, due to high RMS of input current.

Many studies have been presented by the scientific community in order to provide the utilization of AC/DC converters with high power factor for the AC network and low harmonic distortion in the input line current [1, 2, 3]. One of the most employed topologies, but as a pre-regulator, is the Boost converter [1]. This structure is not a naturally isolated and operates only as step-up voltage. The converter proposed in [2] has a good performance, but the structure consists of three synchronized switches, three Y-connected Buck-Boost inductors and another complementary switch to control the output DC voltage. Moreover, the converter is operated in discontinuous conduction mode (DCM) with high RMS current value. In [3] the main advantages of the scheme are the simplicity and the good performance on the AC side; however, the

converter works in DCM, and presents a high switch stresses.

In this paper, we present an analysis and development of a three-phase input feeding source, high power factor, operating at constant frequency, with a single stage of a power processing, employing the DC/DC Sepic converter (Single Ended Primary Inductance Converter) operating in continuous conduction mode. The structure proposed utilizes only one switch for controlling power flow, making the drive circuit extremely simple, with no need for line filters between the input network and the rectifier and can operate as step-down or step-up voltage. Furthermore, the reduced number of components increases the reliability of the system, making it quite attractive for industrial applications.

## II. PRINCIPLE OF OPERATION

The proposed circuit is shown in Fig. 1.

To simplify the analysis, the following assumptions are made: the operation of the circuit is steady-state, the semiconductors are considered ideal, the transformer is considered by its magnetizing inductance reflected to the primary side, the voltage ripple across the capacitors  $C_1$  and  $C_0$  are considered zero, the line voltage is constant during a switching period and the efficiency of the structure is considered equal to 100%.

By referring the parameters of the converter to the primary side of the transformer we obtain the equivalent circuit shown in Fig. 2, where:

$$R_0 = \left(\frac{N_p}{N_s}\right)^2 \cdot R_0'; \quad C_0 = \left(\frac{N_s}{N_p}\right)^2 \cdot C_0'; \quad V_0 = \frac{N_p}{N_s} \cdot V_0' \quad (1)$$

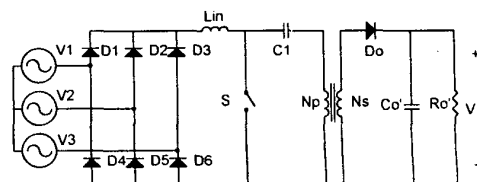


Figure 1: Proposed circuit

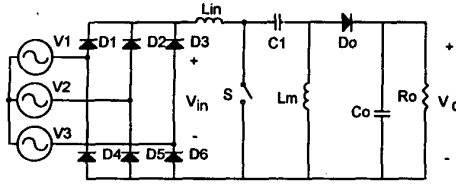


Figure 2: Equivalent circuit with the parameters referred to the primary side.

The Sepic converter working in continuous conduction mode presents two operation stages:

1<sup>st</sup> Stage ( $0 < t < DT$ ) Fig. 3: At moment  $t = 0$ , switch S is turned on. The energy from the source  $V_{in}$  is stored in the inductance  $L_{in}$ , and the capacitor  $C_1$  transfer its energy to the magnetizing inductance  $L_m$ . The capacitor  $C_1$  voltage is considered constant and equal to  $V_{in}$ . The currents  $i_{in}$  and  $i_{Lm}$  increase linearly. During this stage the diode  $D_0$  is kept blocked and the capacitor  $C_0$  supplies energy to the load  $R_0$ .

2<sup>nd</sup> Stage ( $DT < t < T$ ) Fig. 4: At moment  $t = DT$ , switch S is turned off and the diode  $D_0$  is turned on, transferring the inductor storage energy to the load. The currents  $i_{in}$  and  $i_{Lm}$  decrease linearly. The voltage across the switch S is equal to  $(V_{in} + V_0)$ .

The main waveforms are shown in Fig. 5.

### III. MATHEMATICAL ANALYSES

The equations for the functioning of the steady-state Sepic converter operating in CCM are given below:

$$i_{in}(t) = \begin{cases} I_{in0} + \frac{V_{in}}{L_{in}} \cdot t & ; 0 < t < DT \\ \frac{V_{in}}{L_{in}} \cdot DT - \frac{V_0}{L_{in}} (t - DT) + I_{in0} & ; DT < t < T \end{cases} \quad (2)$$

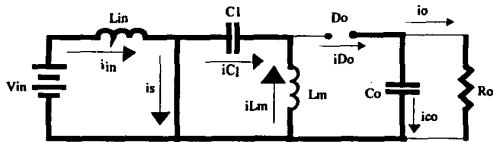


Figure 3: First stage

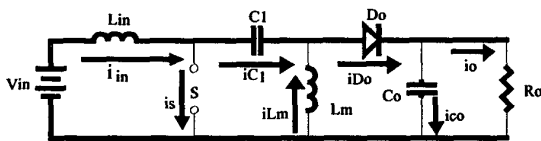


Figure 4: Second stage

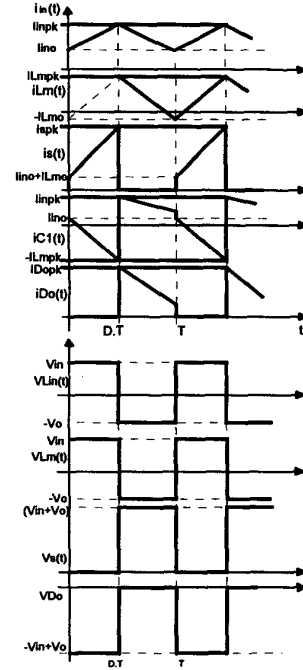


Figure 5: Main waveforms

$$i_{Lm}(t) = \begin{cases} I_{Lm0} + \frac{V_{in}}{L_m} \cdot t & ; 0 < t < DT \\ \frac{V_{in}}{L_m} \cdot DT - \frac{V_0}{L_m} (t - DT) + I_{Lm0} & ; DT < t < T \end{cases} \quad (3)$$

$$i_s(t) = \begin{cases} \frac{V_{in}}{L_{eq}} \cdot t + I_{in0} + I_{Lm0} & ; 0 < t < DT \\ 0 & ; DT < t < T \end{cases} \quad (4)$$

$$i_{C1}(t) = \begin{cases} -\frac{V_{in}}{L_m} \cdot t - I_{Lm0} & ; 0 < t < DT \\ \frac{V_{in}}{L_{in}} \cdot DT - \frac{V_0}{L_{in}} (t - DT) + I_{in0} & ; DT < t < T \end{cases} \quad (5)$$

$$i_{D0}(t) = \begin{cases} 0 & ; 0 < t < DT \\ \frac{V_{in}}{L_{eq}} \cdot DT - \frac{V_0}{L_{eq}} (t - DT) + I_{in0} + I_{Lm0} & ; DT < t < T \end{cases} \quad (6)$$

$$V_{L_{in}}(t), V_{L_m}(t) = \begin{cases} V_{in} & ; 0 < t < DT \\ -V_0 & ; DT < t < T \end{cases} \quad (7)$$

$$V_S(t) = \begin{cases} 0 & ; 0 < t < DT \\ V_{in} + V_0 & ; DT < t < T \end{cases} \quad (8)$$

$$V_{D_0}(t) = \begin{cases} -(V_{in} + V_0) & ; 0 < t < DT \\ 0 & ; DT < t < T \end{cases} \quad (9)$$

Were:  $L_{eq} = \frac{L_{in} \cdot L_m}{L_{in} + L_m}$  ;  $V_{in} = 2.34 \cdot V_{1RMS}$   
DT: Switch  $S_1$  conduction time.

From the input current ripple  $\Delta i_{in}$  and the magnetizing current ripple  $\Delta i_{Lm}$  (Fig. 6), the average and the RMS currents through the components of the Sepic converter can be obtained [4]:

\* Input and switch average currents:

$$I_{in_{av}} = I_{S_{av}} = \frac{V_{in} \cdot DT}{2 \cdot \Delta I_{in} \cdot L_{in}} ; \quad \overline{\Delta I_{in}} = \frac{\Delta I_{in}}{2} \quad (10)$$

\* Average current through the diode "D<sub>0</sub>" and the magnetizing inductance "L<sub>m</sub>":

$$I_{D_{0_{av}}} = I_{L_{m_{av}}} = \frac{V_0 \cdot (1-D) \cdot T}{2 \cdot \Delta I_{Lm}} ; \quad \overline{\Delta I_{Lm}} = \frac{\Delta I_{Lm}}{2} \quad (11)$$

\* Rectifier diodes average current:

$$I_{D_{R_{av}}} = \frac{I_{in_{av}}}{3} \quad (12)$$

\* Input RMS current:

$$I_{in_{RMS}} = \frac{\sqrt{3}}{3} \cdot \frac{V_{in} \cdot DT}{2 \cdot \Delta I_{in} \cdot L_{in}} \cdot \sqrt{3 + (\overline{\Delta I_{in}})^2} \quad (13)$$

\* Switch "S" RMS current:

$$I_{S_{RMS}} = \frac{\sqrt{3}}{3} \cdot \frac{V_{in} \cdot DT}{2 \cdot \Delta I_{in} \cdot L_{in}} \cdot \frac{\sqrt{[D \cdot \overline{\Delta I_{in}} + (1-D) \cdot \overline{\Delta I_{Lm}}]^2 + 3}}{\sqrt{D}} \quad (14)$$

\* Capacitor "C<sub>t</sub>" RMS current:

$$I_{C_{RMS}} = \frac{V_{in} \cdot \sqrt{D} \cdot T}{2 \cdot \Delta I_{in} \cdot L_{in}} \cdot \sqrt{(1-D) \cdot [D \cdot (\overline{\Delta I_{in}})^2 + (1-D) \cdot (\overline{\Delta I_{Lm}})^2 + 3]} \quad (15)$$

\* Diode "D<sub>0</sub>" RMS current:

$$I_{D_{0_{RMS}}} = \frac{V_0 \cdot \sqrt{(1-D)} \cdot T}{2 \cdot \sqrt{3} \cdot \Delta I_{Lm} \cdot L_m} \cdot \sqrt{[D \cdot \overline{\Delta I_{in}} + (1-D) \cdot \overline{\Delta I_{Lm}}]^2 + 3} \quad (16)$$

\* Capacitor "C<sub>0</sub>" RMS current:

$$I_{C_{0_{RMS}}} = \frac{V_0 \cdot (1-D) \cdot T}{2 \cdot \Delta I_{Lm} \cdot L_m} \cdot \sqrt{\frac{[D \cdot \overline{\Delta I_{in}} + (1-D) \cdot \overline{\Delta I_{Lm}}]^2 + 3}{3 \cdot (1-D)}} \quad (17)$$

\* Rectifier diodes RMS current:

$$I_{D_{R_{RMS}}} = \frac{\sqrt{3 + (\overline{\Delta I_{in}})^2}}{3} \cdot I_{in_{av}} \quad (18)$$

\* Input RMS current:

$$I_{in_{RMS}} = \sqrt{2} \cdot \frac{\sqrt{3 + (\overline{\Delta I_{in}})^2}}{3} \cdot I_{in_{av}} \quad (19)$$

From the conservation of the transformer magnetic flux in steady-state condition, we have:

$$V_{in} \cdot DT = V_0 \cdot (1-D) \cdot T \quad (20)$$

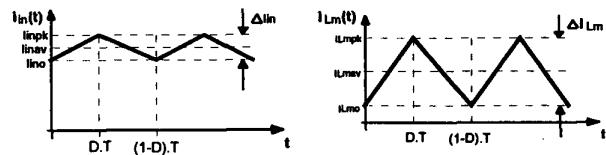


Figure 6: Input and magnetizing currents of the Sepic converter.

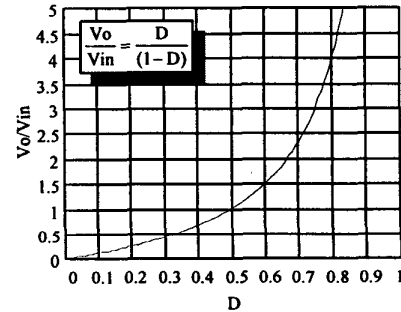


Figure 7: Static gain.

Thus, the characteristic of the static gain of the Sepic converter in CCM, shown in Fig. 7, is given by:

$$\frac{V_0}{V_{in}} = \frac{D}{(1-D)} \quad (21)$$

Fig. 8 shows the external characteristics of the Sepic converter in steady-state [4]. From this figure we can obtain the current value of the critical load that delimits the continuous and discontinuous modes.

#### IV. DESIGN PROCEDURE AND EXAMPLE [4]

From the equations presented in the previous item, it is possible to generate normalized curves that simplify the converter design. These curves, along with the design-procedure, are presented below.

##### A. Input Data

- RMS input phase voltage ( $V_{RMS} = 74V$ )
- Output voltage ( $V_0 = 60V$ )
- Output power ( $P_0 = 600W$ )

- Switching frequency ( $f_s = 20\text{kHz}$ )
- Normal duty cycle ( $D = 0.4$ )
- Efficiency ( $\eta = 80\%$ )

### B. Current Ripple of the Input Inductor ( $\overline{\Delta I_{in}}$ )

The power factor (PF) and the total harmonic distortion (THD) of the converter input current, are directly affected by current ripple of the input inductor. Therefore, to obtain a power factor above 95% and a THD near 30%, we must choose a current ripple  $\overline{\Delta I_{in}}$  below 10%. In this design it was adopted  $\overline{\Delta I_{in}} = 2,5\%$  (see Fig. 9 and 10).

### C. Transformer Ratio (a)

The transformer ratio is given by:

$$a = \frac{V_{in} \cdot D}{V_0 \cdot (1-D)} = \frac{2.34 \cdot 74 \cdot 0.4}{60 \cdot (1-0.4)} \cong 2 \quad (22)$$

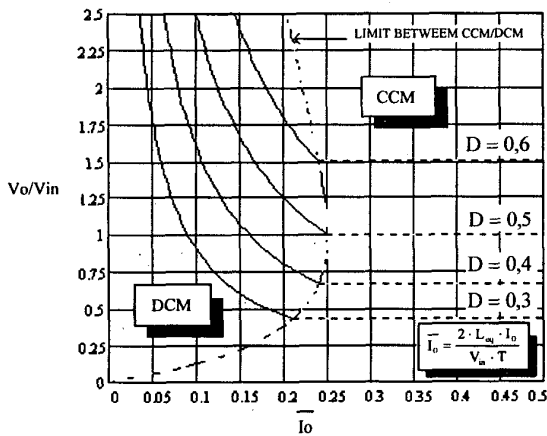


Figure 8: External characteristics of the Sepic converter.

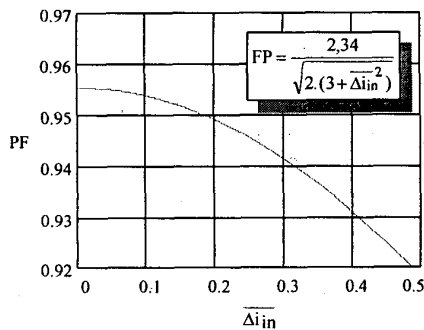


Figure 9: PF vs  $\overline{\Delta I_{in}}$

### D. Input Average current ( $I_{in,av}$ )

The input average current is given by the following equation:

$$I_{in,av} = \frac{P_0}{\eta \cdot V_{in}} = \frac{600}{0.80 \cdot 2.34 \cdot 74} \cong 4.3\text{A} \quad (23)$$

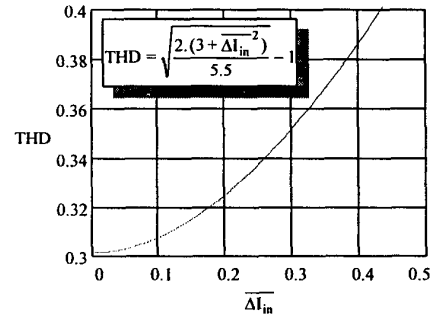


Figure 10: THD vs  $\overline{\Delta I_{in}}$

### E. Input Inductor ( $L_{in}$ )

For that purpose, we adopted 2,5% as input current ripple ( $\overline{\Delta I_{in}}$ ). Therefore:

$$L_{in} = \frac{V_{in} \cdot D}{2 \cdot \overline{\Delta I_{in}} \cdot I_{in,av} \cdot f_s} = \frac{2.34 \cdot 74 \cdot 0.4}{2 \cdot 0.025 \cdot 4.3 \cdot 20\text{k}} \quad (24)$$

$$L_{in} = 16.1\text{mH}$$

### F. Equivalent Inductance ( $L_{eq}$ ) and Magnetizing Inductance ( $L_m$ )

For the calculation of the magnetizing inductance, it is necessary to define the maximum load resistance that guarantees the continuous conduction mode of the converter. From Fig. 8 we can observe that the value of the critical normalized load current, for  $D = 0.4$ , is approximately equal to 0.24. In the Eq. 25 the value of  $\overline{I_0}$  is adopted to be equal to 6 (six) times the critical normalized load current. Thus, we have:

$$L_{eq} = \frac{V_{in} \cdot V_0 \cdot a \cdot \overline{I_0}}{2 \cdot f_s \cdot P_0} = \frac{2.34 \cdot 74 \cdot 60 \cdot 2 \cdot 6 \cdot 0.24}{2 \cdot 20,000 \cdot 600} \quad (25)$$

$$L_{eq} = 1.25\text{mH}$$

From the relation:  $L_{eq} = \frac{L_{in} \cdot L_m}{L_{in} + L_m}$ ; the magnetizing inductance can be obtained:

$$L_m = 1.35\text{mH}$$

### G. Capacitor $C_1$ and Output Capacitor ( $C_0$ )

For both capacitors a voltage ripple of 1% was adopted. Thus:

$$C_1 = \frac{D^2 \cdot P_0}{\Delta V_{C_1} \cdot (1-D) \cdot V_0^2 \cdot f_s \cdot a^2} = \frac{0.4^2 \cdot 600}{0.01 \cdot (1-0.4) \cdot 60^2 \cdot 20,000 \cdot 2^2} \quad (26)$$

$$C_1 \cong 55,56 \mu\text{H}$$

$$C_0 = \frac{D^2 \cdot V_{in} \cdot P_0}{\Delta V_{C_0} \cdot V_0^3 \cdot (1-D) \cdot f_s \cdot a} = \frac{0.4^2 \cdot 2.34 \cdot 74 \cdot 600}{0.01 \cdot 60^3 \cdot (1-0.4) \cdot 20,000 \cdot 2} \quad (27)$$

$$C_2 \cong 320 \mu\text{H}$$

Figs. 11 and 12 show the normalized RMS currents through the capacitors. From Fig. 11 we can obtain the RMS current in the capacitor "C<sub>1</sub>", for  $D = 0.4$ . The same procedure can

be applied for the output capacitor “C<sub>0</sub>” from Fig. 12. Therefore:

$$I_{C1_{RMS}} = 1.25 \cdot I_{in_{av}} = 1.25 \cdot 4.3 = 4.37A \quad (28)$$

$$I_{C0_{RMS}} = 0.83 \cdot I_0 = 0.83 \cdot 10 = 8.3A \quad (29)$$

**H. Choice of the Semiconductors**

From Eqs. (10), (11), (12), (14), (16) and (18), the curves presented in Figs. (13), (14) and (15) can be made; and these figures help us in the choice of the semiconductors. Consequently, from Fig. 13, for D = 0.4, peak and the RMS current through the switch’s can be obtained:

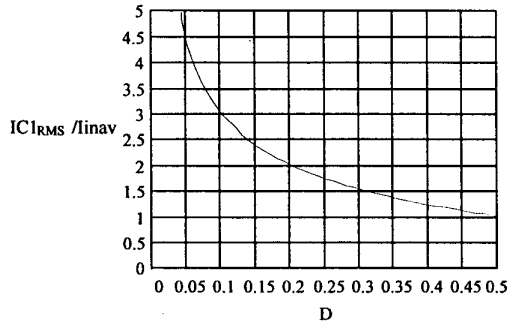


Figure 11: Normalized RMS current in the capacitor C<sub>1</sub>.

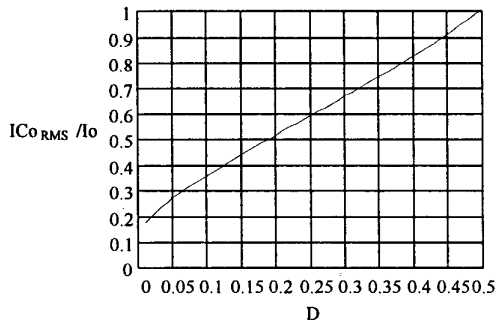


Figure 12: Normalized RMS current in the capacitor C<sub>0</sub>.

$$\begin{cases} I_{SPK} = 3.0 \cdot I_{in_{av}} = 3.0 \cdot 4.3 = 12.9A & (30) \\ I_{SRMS} = 1.6 \cdot I_{in_{av}} = 1.6 \cdot 4.3 = 6.8A & (31) \end{cases}$$

By applying the same strategy to Figs. 14 and 15 it is possible to obtain, respectively, the following results:

$$\begin{cases} I_{D0_{pk}} = 1.88 \cdot I_0 = 1.88 \cdot 10 = 18.8A & (32) \\ I_{D0_{RMS}} = 1.3 \cdot I_0 = 1.3 \cdot 10 = 13A & (33) \end{cases}$$

$$\begin{cases} I_{DR_{PK}} = 3.1 \cdot I_{DR_{av}} = 3.1 \cdot 1.17 = 3.62A & (34) \\ I_{DR_{RMS}} = 1.74 \cdot I_{DR_{av}} = 1.74 \cdot 1.17 = 2.03A & (35) \end{cases}$$

Note: with this design procedure we can obtain all the power circuit components of the three-phase rectifier.

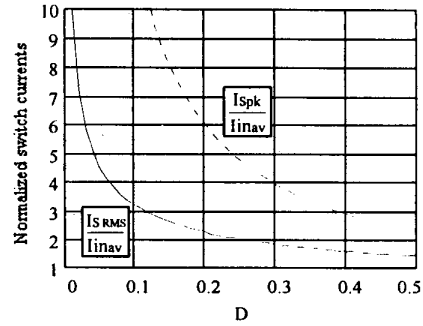


Figure 13: Peak and RMS normalized current in the switch “S”.

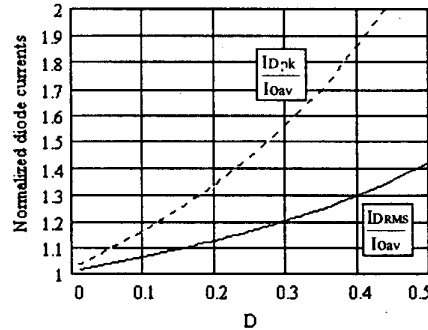


Figure 14: Peak and RMS normalized current in the diode “D<sub>0</sub>”.

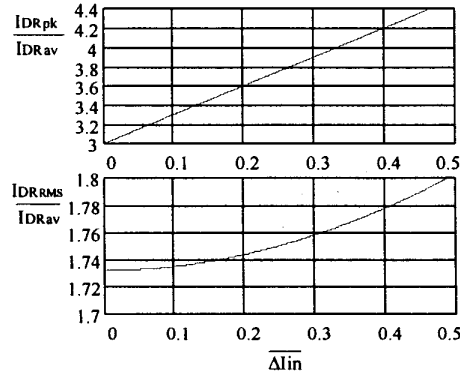


Figure 15: Peak and RMS normalized current in the rectifier diodes.

**V. EXPERIMENTAL RESULTS**

A prototype rated 600W was built to evaluate the proposed circuit [4]. The main specifications were given in the previous item. All the results presented in this work were obtained for full load conditions and the output voltage was kept constant, equal to 60V. Fig. 16 shows the voltage and the current of phase “1”. In Fig. 17 it is shown the waveforms of the voltage and current in the main switch.

Fig. 18 presents the voltage and the current in the diode “D<sub>0</sub>”. The input inductor current is shown in Fig. 19. The power factor (PF) and the total harmonic distortion (THD) are shown in Figs. 20 and 21, respectively. For the full load conditions the power factor obtained was above 0.96 and the THD was 26%. For the same conditions the efficiency ( $\eta$ ) obtained was about 80% (Fig. 22). The main causes of the losses were: magnetic components, output rectifier and hard switching.

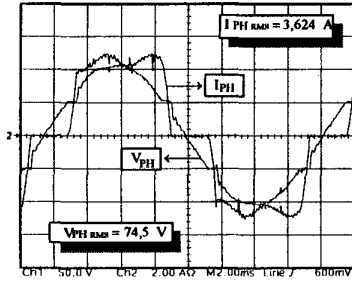


Figure 16: Voltage and current of phase “1”.  
Scale: 50V/div; 2A/div; 2ms/div

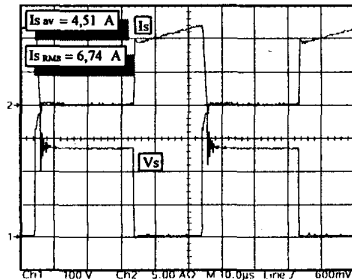


Figure 17: Voltage and current in the main switch.  
Scale: 100V/div; 5A/div; 10 $\mu$ s/div

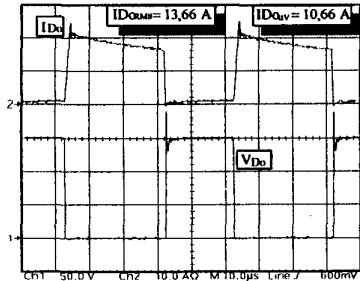


Figure 18: Voltage and current in the diode “D<sub>0</sub>”.  
Scale: 50V/div; 10A/div; 10 $\mu$ s/div

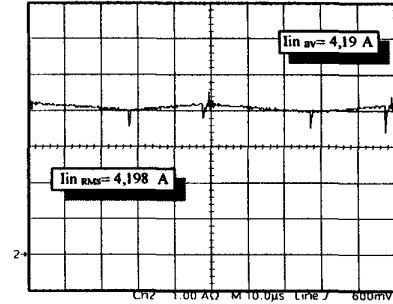


Figure 19: Input inductor current.  
Scale: 1A/div; 10 $\mu$ s/div

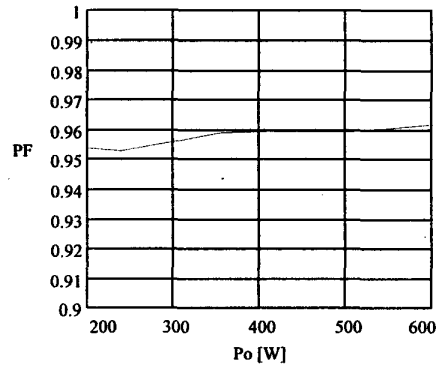


Figure 20: Power factor behavior.

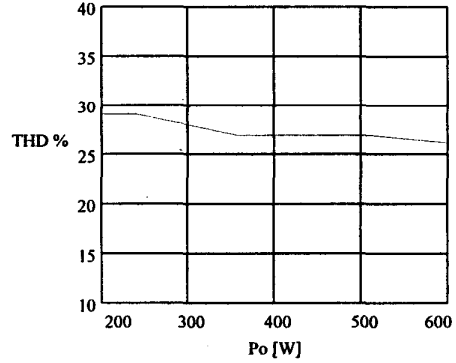


Figure 21: Total harmonic distortion.

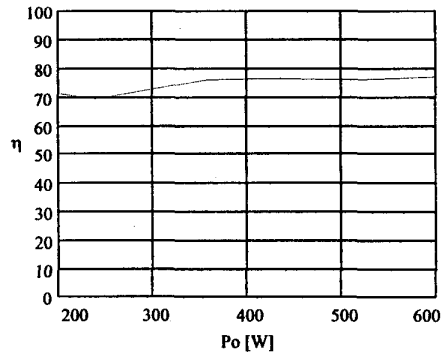


Figure 22: Efficiency of the prototype.

## VI. CONCLUSION

The three-phase rectifier using a Sepic DC-DC converter, has proved to be very robust and easy implementation. The fact that there is only one switch to control the power flow makes for a considerably simplified circuit. In the prototype implemented, only one integrator was used to control the static voltage gain. The reduced number of components and the simplicity of its structure increase its reliability and make it extremely desirable for industrial applications.

This structure is particularly used in applications where the load acts as a source voltage. According to the results obtained we have an AC-DC converter with the following features:

- It is particularly simple and robust;
- It provides power factor correction operating in continuous conduction mode and is therefore more suitable for high power applications;
- It is naturally isolated;
- It has only one controlled switch;
- It operates either as step-up or step-down voltage;
- It can allow a regulated output voltage with only one power processing stage.

Finally, the proposed structure can be utilized at higher power rates without any difficulty.

## REFERENCES

- [1] A. R. Prasad, P.D. Ziogas and S. Manias. "An Active Power Factor Correction Technique for Three Phase Diode Rectifiers". Proc. IEEE - PESC'89, pp. 58-65.
- [2] C. T. Pan & T.C. Chen. "Step-up/down Three Phase AC to DC Converter with Sinusoidal Input Current and Unity Power Factor". IEEE Proc. Electron. Power Appl., Vol. 141, n° 2, pp. 52-77, March 1994.
- [3] L. Malesani et al. "Single-Switch Three-Phase AC/DC Converter with High Power Factor and Wide Regulation Capability". Proc IEEE - PESC92', pp. 279-285, June/1992.
- [4] A.H. Oliveira. "Three-Phase Rectifier with High Power Factor Using a Continuous Conduction Mode Sepic DC-DC Converter". Master Thesis, INEP/EEL/UFSC, Florianópolis-SC-Brasil, 1996 (in Portuguese).