

A PASSIVE LOSSLESS SNUBBER FOR THE HIGH POWER FACTOR UNIDIRECTIONAL THREE-PHASE THREE-LEVEL RECTIFIER

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Abstract – This paper presents a version for three-phase three-level unidirectional rectifier employing a passive lossless snubber. The proposed rectifier operates with soft commutation without the employment of auxiliaries switches. As a consequence, its efficiency is high and its cost is low. Circuit operation, theoretical analysis, design procedure and experimental results are presented.

I. INTRODUCTION

Nonlinear loads, including rectifiers used in telecom power supplies, generate harmonic distortion in the input current and, through the impedance of the line, lead to distortion of the line voltage and contribute to power quality problems.

The main contributions of power supplies to power quality problems are increased current and voltage distortion, sags, common-mode and differential-mode EMI. These problems can lead to failures, reduced hold-up-time, increased output noise and increased cost. In another devices and systems, voltage and current distortion can cause excess audio noise and overheating of transformers, generators and motors, mechanical oscillations in generators and motors, electrical resonance in the distribution system and equipment malfunction [1].

Telecom power supplies have a much greater local impact on power quality, because it usually operates with relatively high power level, has continuous operation and small current variations in the load current.

Availability and energy conversion efficiency are very important since uninterrupted service, continuous operation and high power level are required in a telecom power supply.

Due to the problems and requirements above mentioned, a large potential market, increasingly restricted regulations (IEC 1000-3-2, IEEE 519) and severe economical restraints, power factor correction

rectifiers design has become a focus of attention in the literature.

High frequency unidirectional PWM rectifiers for feeding the DC link of the telecom power supply, must present the following requirements [2]:

- High quality for mains current;
- Lower blocking voltage and current stress on the power semiconductor devices;
- High power density;
- High reliability and efficiency;
- Lower complexity of the power and control circuits.

A large variety of three phase high power factor switched mode rectifiers are presented on the literature. The authors believe that the three-phase three-level rectifier is the best alternative for telecom applications [3] [4]. This topology presents features that are required for telecom applications.

As all boost based converters, in the three phase three-level rectifier substancial power dissipation occurs in the switch because it is subjected simultaneously to increasing current and full output voltage, during turn on commutation. Besides, the reverse recovery mechanism in the diode produces high di/dt and high current peak through the switch.

This problem can be solved by the introduction of a snubber circuit to limit di/dt and dv/dt in the switches and to reduce commutation losses.

To preserve simplicity, robustness, low cost and high efficiency a passive lossless snubber [5] must be associated to the rectifier. Another advantage is that snubber circuits can reduce EMI caused by the switching action in the converter.

This paper introduces a version for three-phase three-level rectifier with passive lossless snubber. The rectifier and the passive lossless snubber (thin line)

are shown in Fig. 1. Principle of operation, circuit description and design considerations for this converter are described in following sections.

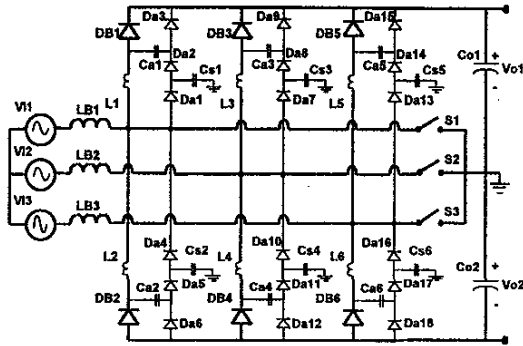


Fig. 1. Three-phase three level rectifier with passive lossless snubber.

II. PRINCIPLE OF OPERATION AND CIRCUIT DESCRIPTION

A. Principle of Operation

Three voltage-doubler rectifiers associated in a *wye* connection can be used for realization of the three phase three level rectifier. A voltage-doubler rectifier, which is shown in Fig. 2, can be advantageous to analyze the principle of operation of the lossless passive snubber circuit associated with the rectifier.

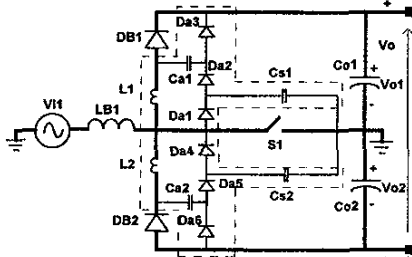


Fig. 2. Voltage doubler rectifier with a passive lossless snubber.

The main requirements of the turn-on snubber are to slow the switch current rise time and to reduce losses. This is possible through the insertion of an inductor into the circuit. From a hard commutation switched converter topology, an inductor is placed in a loop comprised of S1, DB1 (DB2), Co1 (Co2). Thus, when S1 is turned on the output voltage V_{o1} is applied over L1, then the switch current rises with a controllable slope while the voltage remains zero.

To obtain zero voltage turn-off of the switch and controllable voltage slope, it is necessary to include a capacitor into the circuit. When the switch turns off its current is commuted to an auxiliary diode Da1 (Da4) that leads the input current through Cs1 (Cs2). Therefore, the voltage across the switch rises slowly.

Ca1 (Ca2) is used to collect the reverse recovery current energy from L1 (L2) and the energy stored in Cs1 (Cs2) each period through the auxiliaries diodes Da1 (Da4) and Da2 (Da5) during turn on interval. This energy is then used to reset the inductor to input current with the excess transferred to the output through the auxiliary diode Da3 (Da6), during the turn off interval.

Ideally, the absorbed power is neither dissipated nor accumulated in the passive components of this snubber.

B. Stages of Operation

The following simplifications are made to the commutation stages analysis:

- The input voltage source V_{i1} and the input inductor $LB1$ are represented by a constant current source, output stages are represented by constant voltage sources and all components are ideal.

Fig. 3 shows the stages of operation for one switching period.

The stages of operation are described below with respective voltage and current for capacitors and inductors. Time interval equation for each stage is also described.

Stage 1 (t_0-t_1): the input current flows through DB1, L1 and energy are transferred to the output voltage V_{o1} .

$$i_L(t) = I \quad (1)$$

$$V_{Ca}(t) = 0 \quad (2)$$

$$V_{Cs}(t) = V_o \quad (3)$$

V_o is the output voltage and I is the input current.

Stage 2 (t_1-t_2): at $t=t_1$ S1 is turned on and the output voltage is applied to L1, therefore current in DB1 decreases at a linear rate. The switch current increases at the same rate.

$$i_L(t) = I - \frac{V_o}{L} \cdot t \quad (4)$$

$$v_{Ca}(t) = 0 \quad (5)$$

$$v_{Cs}(t) = V_o \quad (6)$$

The time length for this stage corresponds to:

$$\Delta t_2 = \frac{L \cdot I}{V_o} \quad (7)$$

Stage 3 (t_2-t_3): when the current through L1 reaches zero, DB1 turns off, Da2 turns on and the Cs1 discharge starts from V_o .

$$i_L(t) = \frac{-V_o}{\omega \cdot L} \cdot \sin(\omega \cdot t) \quad (8)$$

$$v_{Cs}(t) = V_o \cdot \frac{\omega_s^2}{\omega^2} \cdot \left[\cos(\omega \cdot t) + \frac{\omega^2}{\omega_s^2} - 1 \right] \quad (9)$$

$$v_{Ca}(t) = 0 \quad (10)$$

$$\Delta t_3 = \frac{a \cos\left(1 - \frac{\omega^2}{\omega_s^2}\right)}{\omega} \quad (11)$$

Where

$$\omega = \frac{1}{\sqrt{L \cdot C}}, \quad C = \frac{C_s \cdot C_a}{C_s + C_a}, \quad \omega_s = \frac{1}{\sqrt{L \cdot C_s}} \quad (12)$$

Stage 4 (t_3-t_4): L1 transfers energy to Ca1. This stage is over when the current through L1 reaches zero.

$$i_L(t) = \frac{-V_o \cdot \sqrt{2 \cdot \omega_s^2 - \omega^2}}{\omega_s^2 \cdot L} \cdot \cos(\omega_a \cdot t) + \frac{V_o \cdot \omega_a}{\omega_s^2 \cdot L} \cdot \sin(\omega_a \cdot t) \quad (13)$$

$$v_{Ca}(t) = \frac{V_o \cdot \omega_a^2}{\omega_s^2} \cdot \cos(\omega_a \cdot t) + \frac{V_o \cdot \omega_a}{\omega_s^2} \cdot \sin(\omega_a \cdot t) \quad (14)$$

$$v_{Cs}(t) = 0 \quad (15)$$

$$\Delta t_4 = \frac{a \tan\left(\sqrt{\frac{2 \cdot \omega_s^2 - \omega^2}{\omega_a^2}}\right)}{\omega_a} \quad (16)$$

Where

$$\omega_a = \frac{1}{\sqrt{L \cdot C_a}} \quad (17)$$

Stages 2, 3 and 4 comprise the turn on snubbing action.

Stage 5 (t_4-t_5): S1 conducts the input current. In this stage accumulation of energy in the input inductor occurs.

Stage 6 (t_5-t_6): at $t=t_5$ S1 turns off, and the input current flows through Cs1 and the voltage across it rises linearly. The voltage on the switch is the same as in Cs1 with limited dv/dt .

$$v_{Cs}(t) = \frac{I}{C_s} \cdot t \quad (18)$$

$$\Delta t_6 = \frac{C_s \cdot V_o}{I} \cdot \left(1 - \frac{\omega_a}{\omega_s}\right) \quad (19)$$

Stage 7 (t_6-t_7): when the sum of the voltages in Ca1 and Cs1 reaches V_o , Da3 turns on and Cs1 begins its discharge.

$$i_L(t) = I \cdot [1 - \cos(\omega_s \cdot t)] \quad (20)$$

$$v_{Cs}(t) = \frac{I}{C_s \cdot \omega_s} \cdot \sin(\omega_s \cdot t) + V_o - V_o \cdot \frac{\omega_a}{\omega_s} \quad (21)$$

$$\Delta t_7 = \frac{a \sin\left(\frac{V_o \cdot \omega_a \cdot C_s}{I}\right)}{\omega_s} \quad (22)$$

$$v_{Ca}(t_7) = \frac{V_o \cdot \omega_a}{\omega_s} \quad (23)$$

Stage 8 (t_7-t_8): Da2 turns on when V_{Cs1} reaches V_o . One part of the input current flows through Da1 and Da2 and another through L1 and Ca1.

$$i_L(t) = V_o \cdot \frac{\omega_a}{\omega_s} \cdot \sqrt{\frac{C_a}{L}} \cdot \sin(\omega_a \cdot t) \quad (24)$$

$$v_{Ca}(t) = V_o \cdot \frac{\omega_a}{\omega_s} \cdot \cos(\omega_a \cdot t) \quad (25)$$

$$\Delta t_8 = \frac{a \sin\left(\sqrt{\frac{L}{C_a}} \cdot \frac{\omega_s \cdot I}{V_o}\right)}{\omega_a} \quad (26)$$

Stage 9 (t_8-t_9): when the current through L1 equals the input current I , Da1 and Da2 turn off. Ca1 is discharged at linear rate. The stage finishes when the energy remaining in capacitor Ca1 is totally transferred to the output, and diode DB1 turns on.

$$v_{Ca}(t) = \frac{I}{C_a} \cdot t + \frac{1}{\omega_s} \cdot \sqrt{\frac{C_a \cdot V_o^2 \cdot \omega_a^2 - L \cdot I^2 \cdot \omega_s^2}{C_a}} \quad (27)$$

$$\Delta t_9 = \frac{C_a}{I \cdot \omega_s} \cdot \sqrt{\frac{C_a \cdot V_o^2 \cdot \omega_a^2 - L \cdot I^2 \cdot \omega_s^2}{C_a}} \quad (28)$$

The stages described above are valid for the positive semi cycle of the input voltage and current commutation from DB1 to S1 and from S1 to DB1. During the negative semi cycle of the input voltage current commutation occurs from DB2 to S1 and from S1 to DB2 with the same correspondent stages.

Fig. 3 shows the stages of operation for one switching period and fig. 4 shows the main waveforms for commutation analysis

III. DESIGN CONSIDERATIONS

A. Considerations for Correct Operation

For the correct operation of the converter according to the stages described above at a fixed range of input current, the passive elements must be designed as follows:

- In stage 8, the energy accumulated in Ca1 must be sufficient to increase the inductor L1 current to the value of the input current, before V_{Ca1} reaches zero. If this condition is not satisfied the converter will reach the topological stage 8(a) depicted in Fig. 5, where soft switching at turn on is lost. Hence:

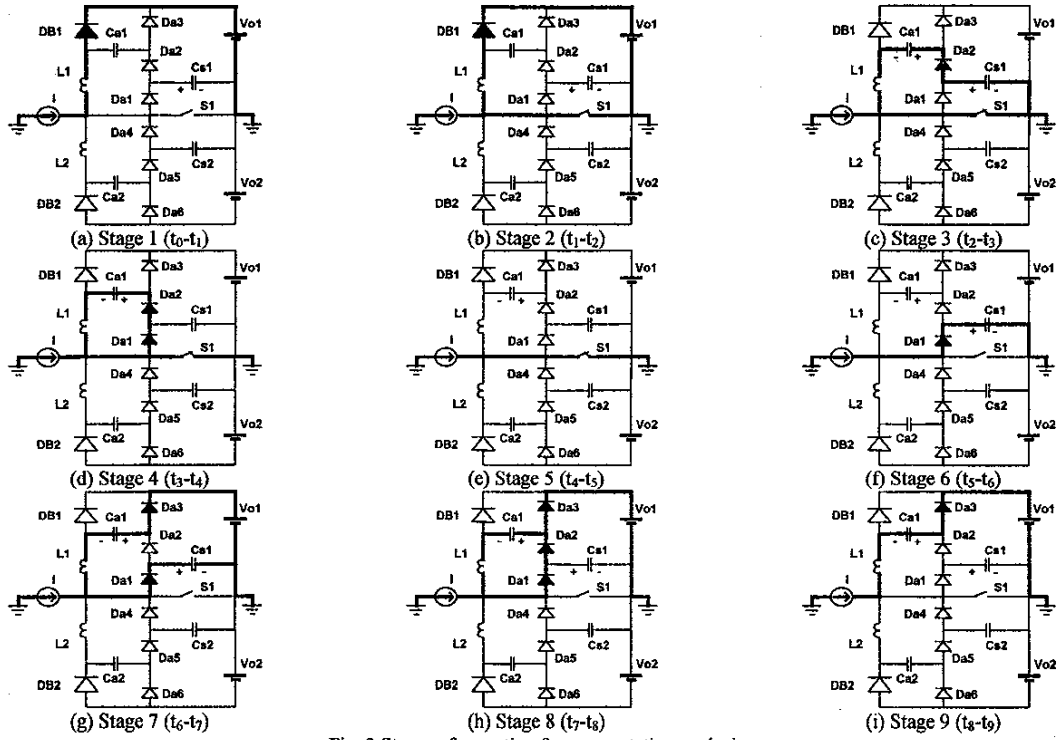


Fig. 3. Stages of operation for commutation analysis

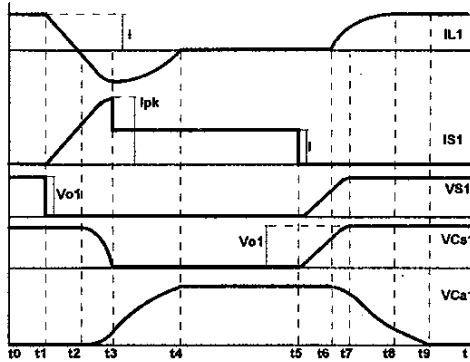


Fig. 4. Waveforms for commutation analysis.

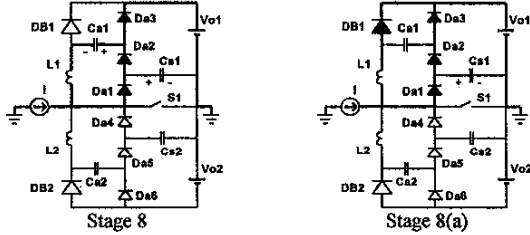


Fig. 5 Undesirable stage

$$\frac{1}{2} \cdot C_a \cdot [V_{Ca}(t_7)]^2 > \frac{1}{2} \cdot L \cdot I^2 \quad (29)$$

Substituting (23) in (29), results in:

$$Z_s = \sqrt{\frac{L}{C_s}} < \frac{V_o}{I} \quad (30)$$

For a given value of Z_s impedance defined by (31), the expression (30) will be valid for any input current below the peak value, assuring soft commutation for any value of input current.

$$Z_s = \sqrt{\frac{L}{C_s}} = \frac{V_o}{I_{max}} \quad (31)$$

• In stage 7, if the inductor current reaches the input current value before the voltage V_{Ca1} reaches the output voltage, the converter may evolve to stage 8(a) as shown in Fig. 5, and therefore the zero current turn on is lost.

From (20), it is established that the inductor current reaches input current at the angle $\omega_s t = \pi/2$. Hence, to satisfy the restriction for stage 7 described above, the voltage across capacitor C_{s1} must be lower than output voltage V_o at the angle $\omega_s t = \pi/2$. Then, from (21):

$$V_o < \frac{I}{C_s \cdot \omega_s} + V_o - V_o \cdot \frac{\omega_a}{\omega_s} \quad (32)$$

$$\frac{V_o}{I \cdot Z_s} < \sqrt{\frac{C_a}{C_s}} \quad (33)$$

Defining the parameter x as the ration between capacitors C_s and C_a , then:

$$x = \frac{C_s}{Ca} \quad (34)$$

In order to ensure soft commutation for a given minimum input current, the parameter x is obtained from (35).

$$\frac{I_{\max}}{I_{\min}} = \sqrt{\frac{1}{x}} \quad (35)$$

The resonant elements are calculated by the (36) and (37).

$$C_s = \frac{1}{Z_s \cdot \omega_s} \quad (36)$$

$$L = \frac{Z_s}{\omega_s} \quad (37)$$

B. Time Interval for Snubber Circuit Operation

In PFC the input current and duty cycle are variable during a main cycle, then the time interval available to stages of operation of snubber circuit is limited as function of the input current and duty cycle.

The time interval for stages 2,3 and 4 must be smaller than the smallest switch conduction time:

$$\Delta_{ton} = \frac{1}{\omega_s} \cdot \left[\frac{I}{I_{\max}} + \frac{a \cos(-x)}{\sqrt{x+1}} + \frac{a \tan\left(\sqrt{\frac{1-x}{x}}\right)}{x} \right] \quad (38)$$

$$\leq T_{sw} \cdot D_{\min}$$

Where T_{sw} is the switching period.

According to (38) the time interval Δt_{on} is proportional to the input current. Hence its maximum value corresponds to the peak input current:

$$\Delta_{ton} = \frac{1}{\omega_s} \cdot \left[1 + \frac{1}{\sqrt{x+1}} \cdot a \cos(-x) + \frac{1}{x} \cdot a \tan\left(\sqrt{\frac{1-x}{x}}\right) \right] \quad (39)$$

$$\leq T_{sw} \cdot D_{\min}$$

$$\omega_s \geq \frac{\left[1 + \frac{1}{\sqrt{x+1}} \cdot a \cos(-x) + \frac{1}{x} \cdot a \tan\left(\sqrt{\frac{1-x}{x}}\right) \right]}{D_{\min} \cdot T_{sw}} \quad (40)$$

The time interval for stages 6,7,8, and 9 must be smaller than the smallest diode DB1 (DB2) conduction time:

$$\Delta_{toff} = \frac{1}{\omega_s} \cdot \left[\frac{I_{\max}}{I} \cdot (1 - \sqrt{x}) + \frac{1}{\sqrt{x}} \cdot \operatorname{asin}\left(\frac{I}{I_{\max}}\right) + \operatorname{asin}\left(\frac{I_{\max}}{I} \sqrt{x}\right) + \sqrt{\frac{1}{x} \cdot \left(\frac{I_{\max}^2}{I^2} - 1\right)} \right] \quad (41)$$

$$\leq T_{sw} \cdot (1 - D_{\max})$$

When duty cycle is in its maximum, the input current is in its minimum and the time interval Δt_{off} is:

$$\Delta_{toff} = \frac{1}{\omega_s} \cdot \left[\frac{1}{\sqrt{x}} - 1 + \frac{\pi}{2} + \frac{1}{\sqrt{x}} \cdot \operatorname{asin}(\sqrt{x}) + \left(\frac{1}{x} \cdot \sqrt{1-x}\right) \right] \quad (42)$$

$$\leq T_{sw} \cdot (1 - D_{\max})$$

$$\omega_s \geq \frac{\left[\frac{1}{\sqrt{x}} - 1 + \frac{\pi}{2} + \frac{1}{\sqrt{x}} \cdot \operatorname{asin}(\sqrt{x}) + \frac{1}{\sqrt{x}} \cdot \sqrt{1-x} \right]}{T_{sw} \cdot (1 - D_{\max})} \quad (43)$$

The capacitor C_s and inductor L are determined from (36) and (37), using the largest value of the frequency ω_s , obtained from expressions (40) and (43).

IV. DESIGN OBJECTIVES, PROCEDURE AND EXAMPLE

The main design procedure objectives are:

- Ensure soft switch at maximum input current;
- Ensure soft switch at a pre-established input current range (I_{\min} - I_{\max});
- Ensure that the duration of the stages of operations related to the snubber operation do not surpass the maximum allowable time, defined for the chosen input current and associated duty cycle ranges.

To illustrate the design procedure an example is presented in this section, whose main specifications are: input voltage $V_{in} = 220$ V(line-line), output voltage $V_{o1} = V_{o2} = 260$ V, output power: $P_o = 3300$ W, switch frequency: $f_s = 50$ kHz.

Firstly the Z_s impedance is calculated by:

$$Z_s = \frac{V_o}{I_{\max}} = \frac{260}{12.25} = 21.22 \Omega$$

The input current range is defined:

$$I_{\min} = 4 \text{ A} \quad I_{\max} = 12.25 \text{ A}$$

The correspondent duty cycle range is:

$$D_{\min} = 1 - \frac{\sqrt{2} \cdot 127}{260} = 0.30 \quad D_{\max} = 1 - \frac{\sqrt{2} \cdot 127}{260} \cdot \frac{4}{12.25} = 0.77$$

The parameter x is given by:

$$x = \left(\frac{I_{\min}}{I_{\max}}\right)^2 = \left(\frac{4}{12.25}\right)^2 = 0.11$$

The frequency ω_s must satisfy both of the inequalities (40) and (42), then:

$$\omega_s > 1.62 \cdot 10^6 \frac{\text{rad}}{\text{s}}$$

The resonant elements for the snubber circuit are given by:

$$C_s = \frac{1}{21.22 \cdot 1.62 \cdot 10^6} = 29 \text{ nF}$$

$$L = \frac{21.22}{1.62 \cdot 10^6} = 13 \mu\text{H} \quad C_a = \frac{29.5 \cdot 10^{-9}}{0.11} = 263.6 \text{ nF}$$

V. EXPERIMENTAL RESULTS

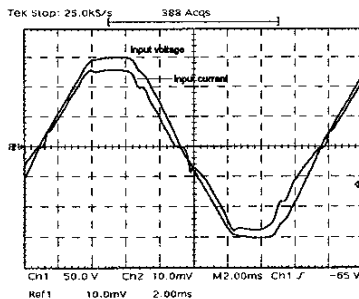
In order to verify the validity of the design procedure and the operation principles, a laboratory prototype has been built.

The power stage of the implemented three-phase converter is depicted in Fig. 2.

Fig. 6 shows the input voltage and current for operation with unity power factor. The details of the turn-on and turn-off commutations operation without snubber circuit are shown in figures (7) and (8) respectively. Clearly the observed commutation are dissipative.

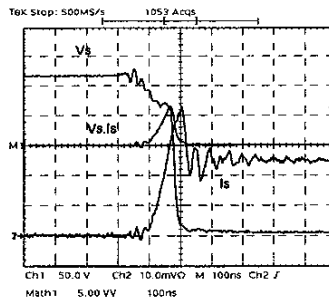
Figures 9 and 10 show the commutations for operation with the snubber circuit, and it is observed that both commutations occur with reduced losses.

The variation of efficiency with respect to output power is shown in Fig. 11.



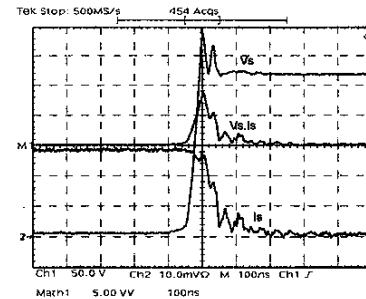
V=50 V/div.; I=5 A/div.; time 2 ms/div..

Fig. 6: Input voltage and current waveforms.



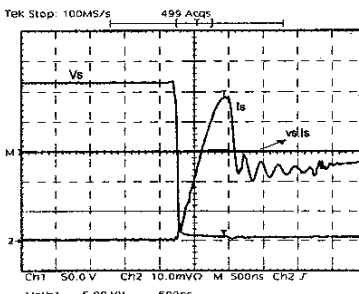
V=50 V/div.; I=5 A/div.; time 100 ns/div..

Fig. 7: Turn-on commutation without snubber.



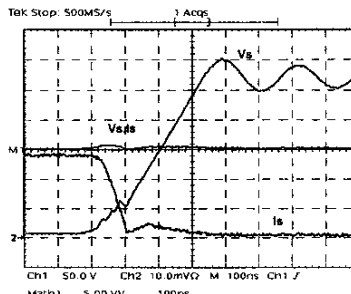
V=50 V/div.; I=5 A/div.; time 100 ns/div..

Fig. 8: Turn-off commutation without snubber.



V=50 V/div.; I=5 A/div.; time 500 ns/div..

Fig. 9: Turn-on commutation with snubber.



V=50 V/div.; I=5 A/div.; time 100 ns/div..

Fig. 10: Turn-off commutation with snubber

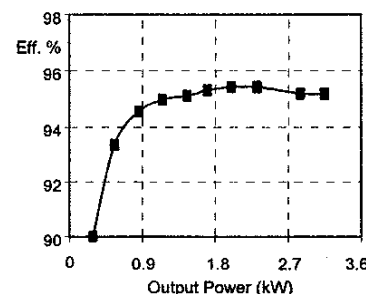


Fig. 11: Efficiency vs. output power.

VI. CONCLUSIONS

The results obtained with the proposed circuit lead to the following conclusions: this paper introduces a version for three-phase three-level rectifier with passive lossless snubber, energy recovery is achieved with passive components only, and experimental waveforms show that the snubber successfully restricts the growth rates of the reverse recovery current and switch voltage.

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