

Reversible Unity Power Factor Step-Up/Step-Down AC–DC Converter Controlled by Sliding Mode

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Abstract—A reversible step-up/step-down ac–dc converter is presented in this paper. It is a fifth-order system, capable of managing power transfer from a dc source to an ac one, with any ratio between the dc and the ac voltage levels, and producing a sinusoidal output current, using only one power processing stage. By reversing the energy flow, this circuit becomes a high power factor rectifier. This reversion can be obtained simply by inverting the reference ac current. The system is analyzed as the connection of two independent lower order subsystems, controlled by sliding mode with decentralised switching scheme. Experimental results from a 100 W prototype operating in both senses, as inverter and as rectifier, are shown to confirm the mathematical analyses and simulations.

Index Terms—AC–DC power conversion, DC–AC power conversion, power quality, power supplies, variable structure systems.

I. INTRODUCTION

THE differential voltage-source inverter, as presented in [1]–[4], is a fourth-order circuit that generates an ac output voltage whose peak value is independent of the dc input level, using only one power processing stage. It is intended mainly for applications requiring peak output voltage higher than the dc input. As it can be seen in Fig. 1, the inverter consists of two independent step-up (or “boost”) converters, each one of them generating a dc-biased sinusoidal voltage. The dc offset is necessary because individual voltages v_{C1} and v_{C2} must be kept higher than V_{in} all the time. Across the load it is applied the differential voltage between the two converters. In this way, if a sinusoidal voltage is desired at the output, the dc levels must be identical, while the ac references for v_{C1} and v_{C2} are phase-shifted (by any angle, although with 180° the best use of the components is achieved).

The goal of the present work is to study this topology acting as an inverter with imposed output current [5], which can be used for ac power (co) generation from photovoltaic cells, for instance. Moreover, by reversing the energy flow, the circuit becomes an ac–dc converter with high power factor input current. The ac current control is made possible by the inclusion of an inductor (L_{ac}) in the original inverter, as shown in Fig. 2, augmenting its total order to five. The current through L_{ac} becomes the variable of major interest, and the difference ($v_{C1} - v_{C2}$) must adapt itself as required by the shape and magnitude of $i_{L_{ac}}$.

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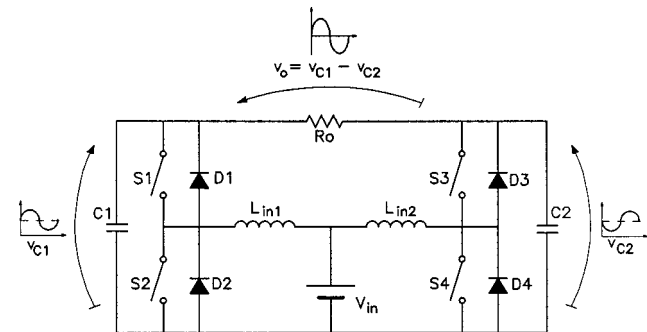


Fig. 1. Diagram of the differential voltage-source inverter implemented with two step-up converters.

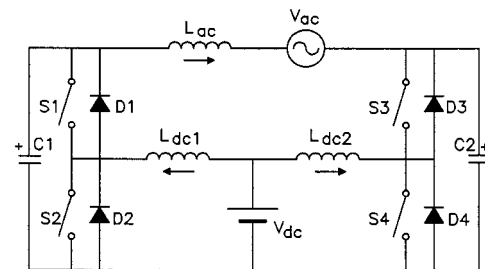


Fig. 2. Circuit of the inverter after insertion of L_{ac} .

Here again, these voltages must never fall below V_{dc} . Due to the possibility of power flow reversion, the sources and inductors are identified as ac or dc, rather than *input* or *output*. The key advantage of the proposed converter is its ability to manage power transfer from a dc source to an ac one with reversibility, irrespective of the ratio between their voltages.

The system is controlled by sliding mode, or sliding regime [6]–[11]. As it is shown in the next sections, two subsystems are defined. They are analyzed separately, governed by independent sliding surfaces, and driven by independent single-input control circuits.

II. ANALYSIS

The complete system can be broken into two parts for control purposes: the “left-side” converter, responsible for controlling $i_{L_{ac}}$, and the “right-side” one, responsible for v_{C2} . These subsystems are coupled, so the output variable of one converter is perceived as a disturbance by the other: $i_{L_{ac}}$ must be imposed through $(v_{ac} + v_{C2})$, and similarly the right-side converter must keep v_{C2} sufficiently close to v_{C2}^* , no matter what the instantaneous value of $i_{L_{ac}}$ is. (Asterisks indicate *reference values*.)

A. Right-Side Converter

Since the right-side converter is a second-order circuit, it is preferable to start the analysis by it. Equation (1) defines the reference for v_{C_2} (ω represents the mains angular frequency)

$$v_{C_2}^*(t) = V_{C_{2dc}}^* + V_{C_{2acp}}^* \cdot \sin(\omega t + \pi). \quad (1)$$

If the voltage v_{ac} is equally divided between capacitors C_1 and C_2 , then each converter processes half of the total output power. So, $V_{C_{2acp}}^* = (1/2) \cdot V_{acp}$, where p stands for *peak value*, and the following condition must be satisfied in excess:

$$V_{C_{2dc}}^* > V_{dc} + \frac{1}{2} \cdot V_{acp}. \quad (2)$$

The step-up configuration requires a duty cycle on S_4 according to (3), here referred to as *right converter duty cycle* (d_R). S_3 , by its turn, receives complementary pulses

$$d_R(t) = 1 - \frac{V_{dc}}{v_{C_2}(t)} \approx 1 - \frac{V_{dc}}{V_{C_{2dc}}^* + \frac{1}{2} \cdot V_{acp} \cdot \sin(\omega t + \pi)}. \quad (3)$$

Current $i_{L_{dc2}}$ for inverter operation can be calculated from the instantaneous energy balance, assuming that, in steady state, all the variables follow their references ($i_{L_{ac}}^*$ is defined in Section II-B)

$$\begin{aligned} i_{L_{dc2}}(t) = & \frac{1}{V_{dc}} \left[\frac{1}{2} \cdot V_{C_{2acp}}^* I_{L_{acp}}^* (1 - \cos 2\omega t) \right. \\ & - V_{C_{2dc}}^* I_{L_{acp}}^* \sin \omega t - \omega C_2 \\ & \left. \cdot \left(V_{C_{2dc}}^* V_{C_{2acp}}^* \cos \omega t - \frac{1}{2} \cdot V_{C_{2acp}}^{*2} \sin 2\omega t \right) \right]. \end{aligned} \quad (4)$$

The above equation describes the low-frequency current through L_{dc2} ; there are still high-frequency excursions due to the commutations between S_3 and S_4 . One observes that there is a continuous term in this current, responsible for the power transfer, added to alternate components of first and second orders. The presence of such components is inherent to the operation of this circuit. If the current through C_2 is negligible, the term $-\omega C_2 \cdot (\dots)$ disappears from (4). In general, i_{C_2} and the switching ripple do not greatly increase the efficient value of the current. In dc-to-ac operation, the positive peak current occurs when $\omega t = 3\pi/2$.

In rectifying operation, all the terms involving $i_{L_{ac}}$ (or $I_{L_{acp}}^*$) in (4) are inverted (in which case the negative peak current occurs at $\omega t = 3\pi/2$). Duty cycle remains unchanged because the reference for v_{C_2} is the same.

Since the gate pulses to the switches are complementary, the discontinuous conduction on L_{dc2} is avoided, and only two subtopologies or structures are possible. They are shown in Fig. 3. S_3, D_3 and S_4, D_4 are presented as single ideal switches, whose state is described by variable γ (5). $i_{L_{ac}}$ is assumed to be at its reference value

$$\begin{cases} \gamma = 1 \Rightarrow S_4, D_4 \text{ ON; } S_3, D_3 \text{ OFF} \\ \gamma = 0 \Rightarrow S_4, D_4 \text{ OFF; } S_3, D_3 \text{ ON} \end{cases}; \quad \bar{\gamma} = (1 - \gamma). \quad (5)$$

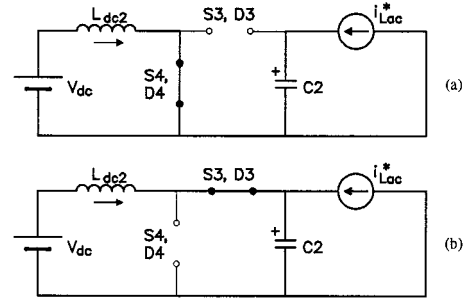


Fig. 3. The two structures of the right-side converter: (a) S_4, D_4 on and (b) S_3, D_3 on.

Situation $\gamma = 1$ is associated to an increase of energy in the circuit. L_{dc2} and C_2 are completely decoupled. The inductor current rises linearly, while $i_{L_{ac}}^*$ flows through C_2 [Fig. 3(a)]. Condition $\gamma = 0$ establishes the coupling between L_{dc2} and C_2 [Fig. 3(b)]. One must observe that $i_{L_{dc2}}$ and $i_{L_{ac}}^*$ can be either positive or negative, depending upon the angle $\varphi = \omega t$.

After defining the error variables $\varepsilon_{v_{C_2}}$ and $\varepsilon_{i_{L_{dc2}}}$ (6), the state error equation (7) can be written. Actually, the low-frequency reference functions, when compared to the switching frequency, can be considered as *quasistatic*, in such a way that the term $(d/dt)[v_{C_2}^*; i_{L_{dc2}}^*]^T$ is, in general, neglected (“ T ” means *transposition*)

$$\varepsilon_{v_{C_2}} = v_{C_2} - v_{C_2}^*; \quad \varepsilon_{i_{L_{dc2}}} = i_{L_{dc2}} - i_{L_{dc2}}^* \quad (6)$$

$$\begin{bmatrix} \varepsilon'_{v_{C_2}} \\ \varepsilon'_{i_{L_{dc2}}} \end{bmatrix} = \begin{bmatrix} i_{L_{dc2}}/C_2 \\ -v_{C_2}/L_{dc2} \end{bmatrix} \cdot \bar{\gamma} + \begin{bmatrix} i_{L_{ac}}^*/C_2 \\ V_{dc}/L_{dc2} \end{bmatrix} - \frac{d}{dt} \begin{bmatrix} v_{C_2}^* \\ i_{L_{dc2}}^* \end{bmatrix}. \quad (7)$$

B. Left-Side Converter

The left-side subsystem is, in fact, a step-up converter with a resonant circuit plus a voltage source at the output. Its main objective (and the objective of the system as a whole) is to control $i_{L_{ac}}$. Any necessary adjustment of the voltage across L_{ac} is done on v_{C_1} , even due to small tracking errors from the right-side converter. The reference for $i_{L_{ac}}$ is defined in inverter mode as a sine function with amplitude $I_{L_{ac}}^*$. For rectifying operation, π rad are added to the argument of the sine function.

The dc offset on the right-side capacitor is naturally established also on C_1 . If this offset is properly chosen, according to (2), both v_{C_1} and v_{C_2} never fall below V_{dc} . Moreover, since L_{ac} is designed to filter the high-frequency switching ripple, its steady-state low-frequency voltage is small, and also the ac component of v_{C_1} oscillates close to $(v_{ac} + v_{C_2})$

$$v_{C_1}(t) \approx V_{C_{2dc}}^* + \frac{1}{2} \cdot V_{acp} \cdot \sin \omega t \quad (8)$$

thus the equations of duty cycle and $i_{L_{dc1}}$ become similar to (3) and (4), respectively, with π rad added to the arguments of each sine or cosine function (or simply the terms in $\sin \omega t$ and $\cos \omega t$ change their signs, while the terms involving $2\omega t$ remain unchanged). Here again, when the system acts as an ac-dc converter, all the terms with $I_{L_{acp}}^*$ are inverted.

The two possible subtopologies for the left-side converter are shown in Fig. 4; it is assumed that v_{C_2} follows exactly its reference. The state of the switches, γ , is defined in (9)

$$\begin{cases} \gamma = 1 \Rightarrow S_2, D_2 \text{ ON}; & S_1, D_1 \text{ OFF} \\ \gamma = 0 \Rightarrow S_2, D_2 \text{ OFF}; & S_1, D_1 \text{ ON} \end{cases}; \quad \bar{\gamma} = (1 - \gamma). \quad (9)$$

Using similar definitions for the error variables as in the previous section, state error equation (10) can be written. The term $d/dt [\dots]^T$ is here neglected

$$\begin{bmatrix} \varepsilon'_{i_{L_{ac}}} \\ \varepsilon'_{v_{C_1}} \\ \varepsilon'_{i_{L_{dc1}}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_{ac}} & 0 \\ -1 & 0 & 0 \\ \frac{C_1}{0} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{L_{ac}} \\ v_{C_1} \\ i_{L_{dc1}} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{i_{L_{dc1}}}{C_1} \\ \frac{-v_{C_1}}{L_{dc1}} \end{bmatrix} \cdot \bar{\gamma} + \begin{bmatrix} \frac{-v_{ac} - v_{C_2}^*}{L_{ac}} \\ 0 \\ \frac{V_{dc}}{L_{dc1}} \end{bmatrix}. \quad (10)$$

III. CONTROL STRATEGY

The system is controlled by sliding mode or sliding regime. A sliding-mode controller changes its structure in order to bring and keep the output close to the desired condition [6]–[11]. It is well suited to power electronics circuits, because they present a particular structure for each state of the switches, naturally changing their structures according to switching actions. The sliding mode takes place in the error state space, in which a trajectory crossing the origin is designed. When the representative point of the system reaches the trajectory, it is confined close to it, and then directed toward the origin of the space. (The origin represents the desired condition: null error.) This trajectory is called *sliding surface* (σ), and the motion, *sliding mode* or *sliding regime*. The designed sliding surface divides the space into two subspaces, each one associated to a structure. One must ensure that the motion in the neighborhood of σ be directed toward the surface, so that the representative point does not deviate from the specified trajectory. This is known as the *existence condition*, mathematically expressed by (17) ($\sigma' = d\sigma/dt$)

$$\lim_{\sigma \rightarrow 0^-} \sigma' > 0 \quad \text{and} \quad \lim_{\sigma \rightarrow 0^+} \sigma' < 0. \quad (11)$$

The practical sliding mode does not occur exactly on the sliding surface all the time, since this would require an infinite switching frequency. In fact, it happens very close to it, giving rise to what is called a *quasisliding mode* [8]. Alternatively, *sliding mode* can be used in generic sense, reserving the expression *limit sliding-mode* for the theoretical case [11]. A simple way to implement the quasisliding mode is by hysteric comparison between the actual state and the desired trajectory.

Equation (12) defines the right-side sliding surface σ_R . It can be regarded as a weighted sum of the errors. Taking s_1 and s_2 constant, the “surface” becomes, in fact, a straight line in the

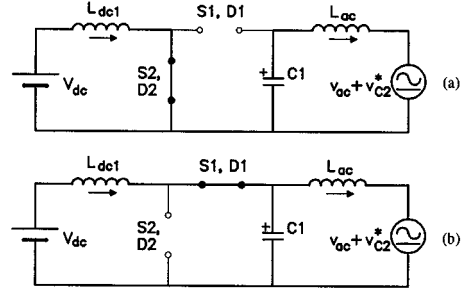


Fig. 4. The two structures assumed by the left-side converter: (a) S_2, D_2 on and (b) S_2, D_2 off.

plane $\varepsilon_{v_{C_2}} \times \varepsilon_{i_{L_{dc2}}}$, completely determined by its slope, $\alpha_R = s_1/s_2$. Units: s_2 in ohms, α in siemens; s_1 is dimensionless

$$\sigma_R = s_1 \cdot \varepsilon_{v_{C_2}} + s_2 \cdot \varepsilon_{i_{L_{dc2}}}. \quad (12)$$

Due to the definition adopted for the error variables (6), whenever the representative point lies below the switching line σ_R , there is little energy in the storing elements C_2 and L_{dc2} , and thus γ is set to 1. Conversely, the subspace above σ_R is associated to surplus energy and to $\gamma = 0$.

From condition (11), one obtains the limits for α_R (13), and also the minimum v_{C_2} for the sliding regime to take place, (14), where $Z_{nR} = \sqrt{L_{dc2}/C_2}$.

$$0 < \alpha_R < \left[V_{dc} \cdot C_2 / \left(L_{dc2} \cdot I_{L_{acp}}^* \right) \right], \quad (13)$$

$$v_{C_2}(t) > V_{dc} + \max\{\alpha_R \cdot Z_{nR}^2 \cdot [i_{L_{ac}}^*(t) + i_{L_{dc2}}(t)], 0\}. \quad (14)$$

Using a fixed hysteresis width $\Delta\sigma_R$, the time interval between two commutations can be obtained through $\Delta t(\gamma) = |\Delta\sigma_R/\sigma'_R|$. By calculating Δt for one hysteresis cycle, making use of expressions (3), (7), and the derivative of (12), an expression for the steady-state switching frequency can be obtained. As it can be seen, it depends on the point of operation (duty cycle and current through L_{ac})

$$f_{sR}(t) = [d_R(t)/\Delta\sigma_R] \cdot [s_2 \cdot V_{dc}/L_{dc2} + s_1 \cdot i_{L_{ac}}^*(t)/C_2]. \quad (15)$$

When $i_{L_{ac}}$ reaches its negative peak value, the variations of $i_{L_{dc2}}$ and v_{C_2} become maximum. In ac-dc operation, this happens at $\varphi = \omega t = \pi/2$ rad, and both duty cycle and switching frequency are at their minimum. So, L_{dc2} and C_2 can be chosen in agreement with (16), and also the hysteresis width must be elected accordingly. Another aspect to be considered when determining C_2 is its low-frequency current, which should not exceed 5% or 10% of rated $i_{L_{ac}}^*$

$$L_{dc2} \geq \frac{V_{dc} \cdot d_{R_{\min}}}{\Delta I_{L_{dc2\max}} \cdot f_{sR_{\min}}} \quad \text{and} \quad C_2 \geq \frac{I_{L_{acp}}^* \cdot d_{R_{\min}}}{\Delta V_{C_2\max} \cdot f_{sR_{\min}}}. \quad (16)$$

The left-side third-order converter requires a bidimensional sliding surface σ_L , defined in (17), as shown at the bottom of

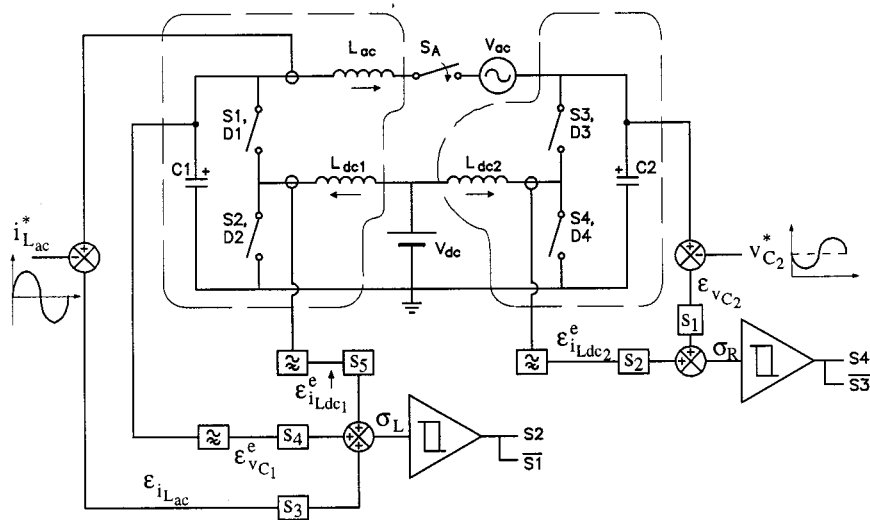


Fig. 5. General portrait of the system. With the decentralized scheme, two sliding surfaces are defined, each one applied to a subconverter.

the page. The selection of s_4 and s_5 follows the same procedure adopted for the right-side sliding-mode controller, using an $\alpha_L = s_4/s_5$, limited in the same way as in (13), and a lower limit for v_{C_1} as in (14). The parameter s_3 is chosen at last, after considering the maximum value of $|v_{L_{ac}}|$, according to (18) shown at the bottom of the page. The evolution of $i_{L_{ac}}(t)$ does not remarkably affect the switching frequency and the duty cycle, so basically the equations for the left side are close to those established for the right side, with a π rad phase-shift. Also (16) is used for sizing L_{dc1} and C_1 .

This way of considering the whole system as the interconnection of two or more subsystems, each one driven by an independent single-input control circuit, is known as *decentralized switching scheme* [8].

As a matter of fact, on the right side, only the reference for the output variable v_{C_2} is explicitly declared, and $\epsilon_{v_{C_2}}$ is denominated the *ruling parameter*; $i_{L_{dc2}}$, here called *secondary variable*, depends upon instantaneous operational conditions and energy demand of the circuit, so its reference is difficult to determine. It is important to observe that, while v_{C_2} governs the converter's macroscopical behavior, the short on and off intervals are mainly dictated by the excursions of $i_{L_{dc2}}$, so that only its sharp, high-frequency trips are necessary to the controller. In this way, signal $\epsilon_{i_{L_{dc2}}}^e$ is actually obtained after a high-pass filtering on the sensed variable (carrying the superscript "e", for "estimated"). The low-frequency $i_{L_{dc2}}$ is assumed to naturally adapt itself to circuit demands. Similarly, on the left side, $\epsilon_{i_{L_{ac}}}$ is the ruling parameter, reference $i_{L_{ac}}^*$ is well defined, while secondary variables v_{C_1} and $i_{L_{dc1}}$ are high-pass filtered.

The use of such high-pass filters is preferred to the use of a calculated reference for the secondary variables, since the controller seeks to nullify the weighted *sum* of errors, and not an error in particular. Thus, if one of those references is wrongly determined, this would result in tracking imperfections in the output variables. This technique is well suited to dc-dc converters [12]–[15]. In the present application, the low-frequency ac evolutions (up to doubled mains frequency) can be considered as quasistatic, therefore allowing the use of the same technique, similarly as it has been shown in [2]–[4], [16], and [17]. Of course the inclusion of each filter contributes to increase the order of the system and in general, during transients, the response becomes more oscillatory than it would be using defined references for the secondary variables. It is desirable to have fast filters, with high cutoff frequency, in order not to alter greatly the dynamics of the circuit, but on the other hand they must present some sensitivity to the resonant frequency of L_{dc1} and C_1 (or L_{dc2} and C_2), remembering that the resonant frequency in a switched circuit depends also on the duty cycle [18]. One must observe that, for safety, a current limitation must be implemented for the dc inductors [12]–[15], because with the filters the system is not sensitive to the value of the current when the switch is on for a long period of time (this is especially true during start-up).

Also the selection of L_{ac} is conditioned by the high-pass filters, especially by the filter for v_{C_1} , which must be sensitive to the resonant frequency between L_{ac} and the series association of C_1 and C_2 .

A general portrait of the converter and its sliding-mode controllers is depicted in Fig. 5. One can see the power circuit, the

$$\sigma_L = s_3 \cdot \epsilon_{i_{L_{ac}}} + s_4 \cdot \epsilon_{v_{C_1}} + s_5 \cdot \epsilon_{i_{L_{dc1}}} \quad (17)$$

$$s_3 \cdot |v_{L_{ac}}| < S_5 \cdot L_{ac} \min \left\{ \left[\frac{V_{dc}}{L_{dc1}} - \frac{\alpha_L \cdot i_{L_{ac}}}{C_1} \right], \left[\frac{v_{C_1} - V_{dc}}{L_{dc1}} + \frac{\alpha_L (i_{L_{ac}} - i_{L_{dc1}})}{C_1} \right] \right\} \quad (18)$$

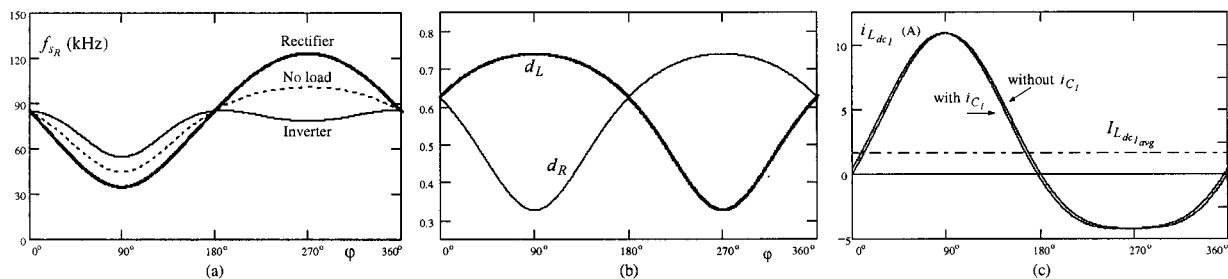


Fig. 6. Theoretical curves: (a) right-side switching frequency regarding the following cases: full-load ac-dc, no-load, and full-load dc-ac operation, (b) duty cycles on both sides (concerning either ac-dc or dc-ac power flow), and (c) current through L_{dc1} for inverter operation (compare to Figs. 7(c) and 10(c)); the positive average current indicates power flowing from the dc source.

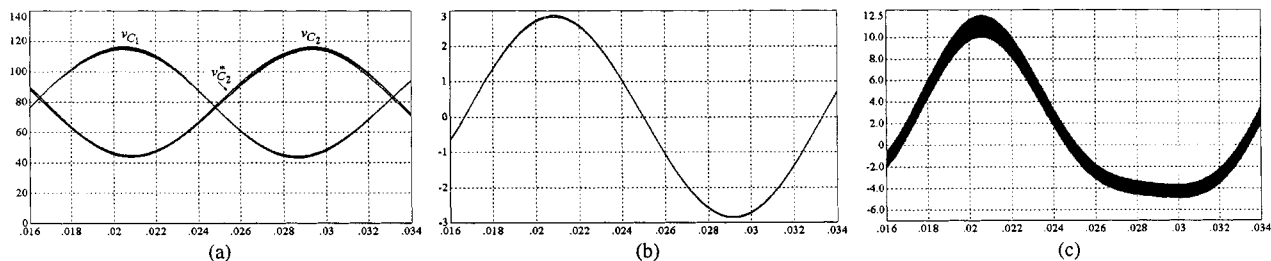


Fig. 7. Simulation results of the converter acting as inverter: (a) v_{C1} and v_{C2} along with v_{C2}^* , (b) i_{Lac} and i_{Lac}^* , and (c) i_{Ldc1} . Vertical scales: (a) volts, (b) and (c) ampères; time in seconds.

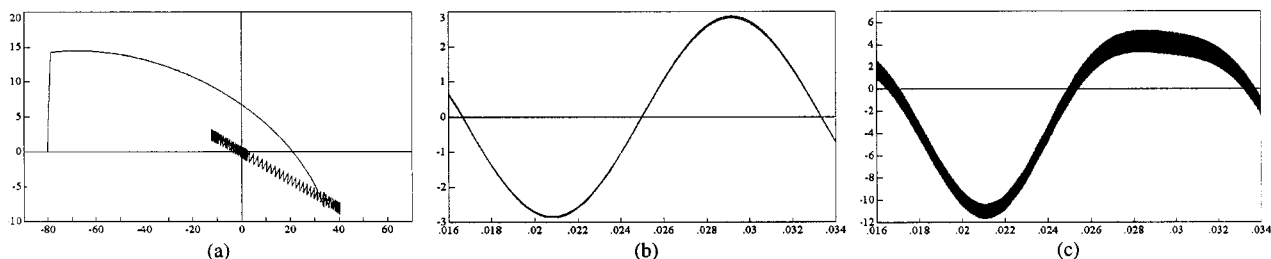


Fig. 8. (a) Right-side state error plane $\varepsilon_{vC2} \times \varepsilon_{iLdc2}^*$, showing start-up from rest, keeping $i_{Lac} = 0$. Simulation results for ac-dc operation. (b) i_{Lac} and i_{Lac}^* . (c) i_{Ldc1} . Horizontal scales: (a) volts, (b) and (c): seconds. Vertical scales: ampères.

signals to be measured, the high-pass filters, the definitions of the surfaces σ_L and σ_R , the hysteretic comparators, and also a sketch of the reference signals to be followed.

During start-up, first the dc value of v_{C2} is established, then S_A is turned on; at last, the ac values (v_{ac} , v_{C2ac}^* , and i_{Lac}^*) are slowly increased.

IV. DESIGN EXAMPLE AND SIMULATION RESULTS

A system was designed to perform 100 W dc-ac and ac-dc power transfer between the sources specified below:

- $V_{dc} = 30$ V;
- $v_{ac}(t) = 70.7 \sin \omega t$;
- $f_{ac} = 60$ Hz.

The reference functions are defined in (19) and (20). (The latter must be shifted by π rad when considering ac-dc operation.) With $V_{C2dc}^* = 80$ V, it is assured at least a 14 V difference between v_{C2} and V_{dc} (and also between v_{C1} and V_{dc}). With this selection of voltages, duty cycles d_R and d_L range from 0.33 to 0.74. Establishing the minimum switching frequency as 35 kHz,

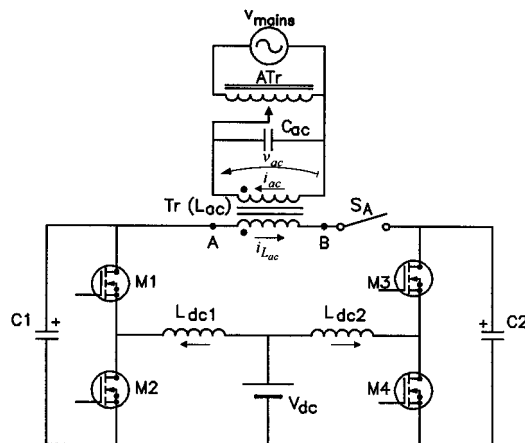


Fig. 9. Diagram of the laboratory prototype.

the passive components result $L_{dc1} = L_{dc2} = 141 \mu\text{H}$ and $C_1 = C_2 = 12 \mu\text{F}$; α must be lower than 0.9 S. In order to

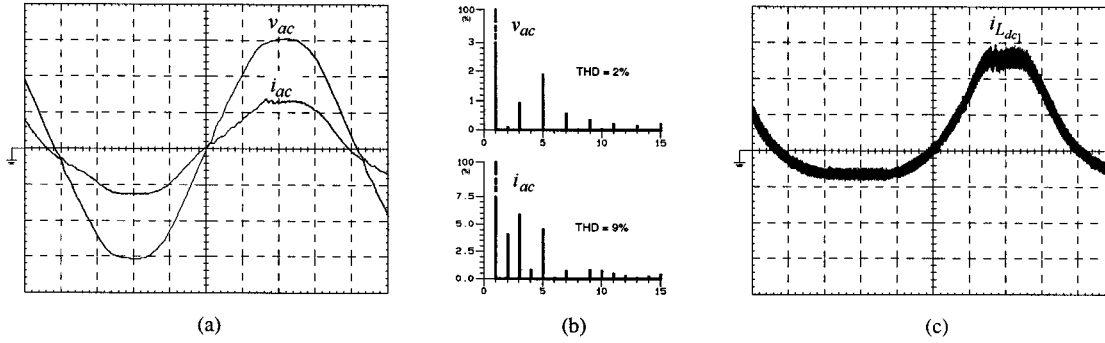


Fig. 10. Experimental results obtained in full-load inverter mode: (a) primary voltage and current (scales: 100 V/div., 500 mA/div., 2 ms/div.), (b) harmonic spectra of v_{ac} and i_{ac} , and (c) current through inductor L_{dc1} (scales: 5 A/div., 2 ms/div.).

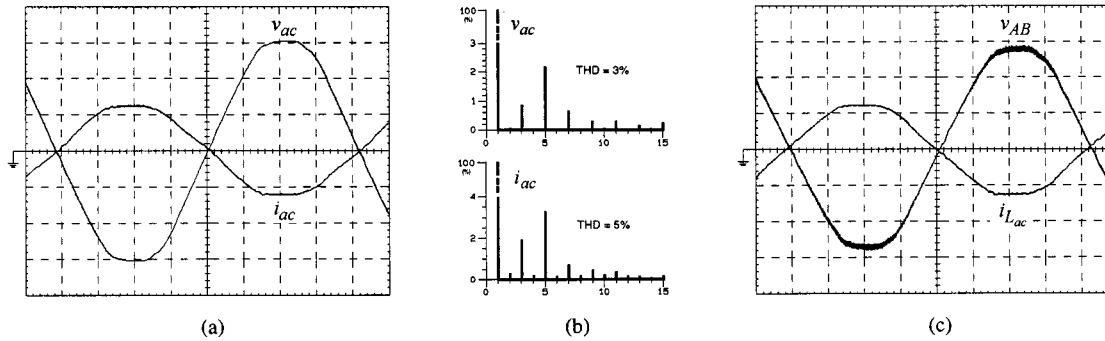


Fig. 11. Experimental results obtained in full-load rectifier operation: (a) primary voltage and current (scales: 100 V/div., 500 mA/div., 2 ms/div.), (b) frequency spectra of v_{ac} and i_{ac} , and (c) secondary voltage and current (scales: 25 V/div., 2 A/div., 2 ms/div.).

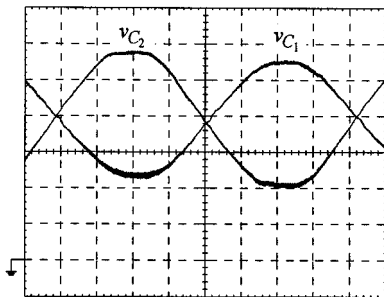


Fig. 12. Voltages across capacitors C_1 and C_2 under full-load rectifier operation. Scales: 20 V/div., 2 ms/div.

have voltages suitable for the control circuit, $s_1 = s_4 = 0.1$ and $s_2 = s_5 = 0.5 \Omega$ are chosen, and thus the maximum switching frequency is found to be 123 kHz (at full-load rectifying operation). Moreover, the total hysteresis width is selected as $\Delta\sigma_R = \Delta\sigma_L 0.78$ V. PL_{ac} is 3.9 mH and s_3 can be safely selected as 1.0Ω . $\varepsilon_{i_{L_{dc2}}}^e$ is obtained from $i_{L_{dc2}}$ through a first-order high-pass filter tuned to 1.5 kHz; a similar filter yields $\varepsilon_{v_{C1}}^e$ from v_{C1} . For $\varepsilon_{i_{L_{dc1}}}^e$, a Butterworth second-order filter tuned to 1.2 kHz is used

$$v_{C2}^*(t) = 80 - 35.4 \sin \omega t \text{ (V);} \quad (19)$$

$$i_{L_{ac}}^*(t) = 2.83 \sin \omega t \text{ (A).} \quad (20)$$

Due to the combination of parameters in (15), the widest variation of the switching frequency occurs under full-load ac–dc operation, becoming minimum under full-load inverter operation, as illustrated in Fig. 6(a) for the right side.

Fig. 6(b) shows the theoretical curves of duty cycles on both sides as functions of $\varphi = \omega t$. They range from 0.33 to 0.78. Theoretical $i_{L_{dc1}}$ for full-load inverter operation can be seen in Fig. 6(c) (excluding high-frequency trips), considering and not considering the current through C_1 . It is interesting to compare this curve to those obtained through simulation [Fig. 7(c)] and experimentation [Fig. 10(c)], noticing that in the latter, $\varphi = 0^\circ$ occurs in the middle of the horizontal axis.

The system was simulated through the program *VisSim*. The main results for inverter mode are shown in Fig. 7. It can be seen from Figs. 7(a) and (b) that v_{C2} and $i_{L_{ac}}$ are sufficiently close to their references. The state error plane of Fig. 8(a) was obtained for the right-side converter starting from rest, i.e., $i_{L_{dc2}}(0) = 0$ and $v_{C2}(0) = 0$, and keeping switch S_A off. There is actually a current limitation at $i_{L_{dc2}} = 20$ A (which corresponds to $\varepsilon_{i_{L_{dc2}}}^e \approx 14$ A). The circuit exhibits an oscillatory transition before reaching the origin. Actually, the right-side subsystem presents a second-order response: there is a reduction of order due to the sliding mode [8], and an increase of order due to the filter. The results for ac–dc operation are shown in Figs. 8(b) and (c).

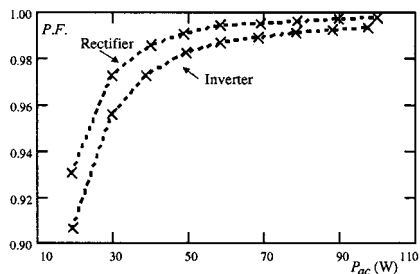


Fig. 13. Variation of the power factor with the ac power.

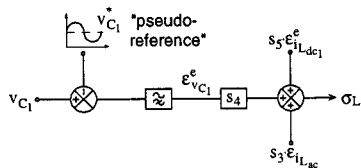


Fig. 14. Use of the pseudo-reference.

V. EXPERIMENTAL RESULTS

In order to verify the operation of the system, a circuit was implemented according to the scheme of Fig. 9. It is intended to be a low-power, low-voltage prototype. For this reason, transformer Tr is used for adapting the mains 220 V_{rms} to the necessary 50 V_{rms} on the secondary side (between points A and B). Its leakage inductance was measured as 3.9 mH on the secondary side; this value is suitable for L_{ac} , so an external inductor is not required. The system is connected to the mains via an autotransformer (ATr). A 12 μ F polypropylene capacitor (C_{ac}) is included in the circuit, so that the leakage inductance of the autotransformer and of the grid do not influence the value of L_{ac} . Mains frequency is 60 Hz. L_{dc1} and L_{dc2} are assembled on Thornton EE 42/15 cores; they were measured respectively as 136 μ H and 153 μ H. Capacitors: $C_1 = 11 \mu$ F; $C_2 = 13 \mu$ F (polypropylene). Main switches are APT 4020 MOSFET's, and V_{dc} is a 30 V power supply. The reference signals v_{C2ac}^* and i_{Lac}^* used in the control circuit are proportional to v_{mains} .

Voltages and currents observed in full-load inverter mode are shown in Fig. 10. It can be seen that v_{ac} itself presents some harmonic distortion, and consequently so does also the reference i_{Lac}^* . The total harmonic distortion of the primary current is 9% and the power factor is 0.997. On the secondary side, i_{Lac} , the actually controlled current, exhibits THD = 5%.

In ac-dc operation, the resulting THD is better: 5% on the primary side of the transformer (4% on the secondary), and the power factor is 0.999. The corresponding curves can be seen in Fig. 11. In Fig. 12, voltages v_{C1} and v_{C2} are shown; the latter is controlled by the right-side converter, keeping at approximately 35 V the peak value of its 60 Hz component. v_{C1} , by its turn, varies according to the operational condition, in such a way that $v_{AB}(=v_{C1} - v_{C2})$ changes from about 66 V at full-load rectifier operation (see Fig. 12) to about 76 V at full-load inverter operation, in order to conform i_{Lac} to its reference, compensating for the voltage drop across L_{ac} and transformer losses.

Fig. 13 illustrates how the power factor varies with the power (measured on the primary side of the transformer), in rectifier

mode and in inverter mode. Under low power conditions, the power factor is more influenced by the magnetizing current of the transformer.

VI. CONCLUSION

The step-up inverter showed to be an interesting way to perform ac-to-dc and/or dc-to-ac power transfer, with no concerns about the relative voltage levels on the dc and the ac sides, using only one power processing stage. The sliding-mode controller with decentralised switching scheme fits very well for this circuit to find and track the time-varying reference functions. These functions are only defined for the two output variables; other signals are high-pass filtered. The use of such filters does not remarkably degrade the overall performance of the system. The transition between rectifier mode and inverter mode is achieved simply by inverting the reference for the ac current. Experimental results shown in the paper corroborate the theoretical predictions. The prototype operates with power factor higher than 0.98 from full-load down to 47% rated power (36% in rectifier mode).

APPENDIX

As it has been stated in the article, the calculated function for v_{C1}^* (8) is not precise. Nevertheless, it can be used as a "pseudo-reference" for v_{C1} , before the high-pass filter, as shown in Fig. 14, aiming to diminish the amount to be filtered, thus increasing the efficiency of the comparison.

In the practical implementation described in Section V, however, it was observed that the power factor obtained without the pseudo-reference is slightly better than that obtained using it. The pseudo-reference does improve the efficiency of the comparison, but the residual error in the filtered v_{C1} helps to compensate for the displacement caused by the magnetizing current of the transformer in the primary i_{ac} current.

The magnetizing current has a leading effect on i_{ac} in inverter operation and a lagging effect in rectifier operation. The 60 Hz component that remains after the first-order filtering acts in the desired sense, i.e., it has a lagging effect in inverter mode, and a leading effect in rectifier mode. In the prototype, this effect produces a displacement of about 3.7° in full-load operation. In this way, the filter cutoff frequency and the gain s_4 can be selected to improve the power factor.

Of course, this result would not be desirable if the system were connected directly to the ac supply. The simulation results of Section IV were obtained *with* the pseudo-reference; the experimental results of Section V were obtained *without* the pseudo-reference, except for the variation of the power factor (Fig. 13).

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