

A Novel Uninterruptible Power Supply System With Active Power Factor Correction

Nimrod Vázquez, *Student Member, IEEE*, Carlos Aguilar, *Member, IEEE*, Jaime Arau, *Senior Member, IEEE*, Ramón O. Cáceres, *Member, IEEE*, Ivo Barbi, *Senior Member, IEEE*, and Jaime Alvarez Gallegos, *Senior Member, IEEE*

Abstract—This paper presents a simplified sinusoidal uninterruptible power supply (UPS) system. The proposed scheme includes features such as high power factor, low total harmonic distortion and good dynamic response at the ac output voltage. In addition, the scheme has the desirable characteristics of high efficiency, simple circuit and low cost compared with a traditional standalone multiple stages UPS with power factor correction. The paper also presents the circuit operation, the analysis and, experimental results of the proposed UPS scheme. The proposed UPS approach is a good solution in low power applications (≤ 500 W).

Index Terms—Battery chargers, boost inverters, power factor correction, uninterruptible power systems, variable structure systems.

I. INTRODUCTION

TO ADD an external UPS is the traditional approach used to provide uninterruptible power in applications such as personal computers, medical equipment, telecommunication systems, control systems, etc. On the other hand, it is desirable to include power factor correction (PFC) because of the well-known advantages that this improvement represents; besides, the international regulations make it mandatory. However, in order to get this capacity, it is necessary to add an extra power stage as can be seen in Fig. 1. In some applications, a sinusoidal output voltage is required, and in those cases, the power inverter stage is implemented based on the full-bridge buck inverter (FB-BI). In these converters, the output voltage is always lower than the dc input voltage; therefore, it is necessary to add an extra stage or a transformer to adequate its input voltage (Fig. 1).

As it can be observed in Fig. 1, the UPS scheme consists of four power conversion stages, resulting poor efficiency, high

cost and low reliability. In this paper, a novel scheme of an uninterruptible power supply system based on two power conversion stages is presented. The proposed configuration has low weight, high efficiency and low cost. Besides, it exhibits close unity power factor.

II. PROPOSED SYSTEM

Fig. 2 shows the proposed UPS, which is based on two power conversion stages. The UPS offers excellent features, such as: simple structure, high power factor, low total harmonic distortion (THD), fast dynamic response at the output voltage, high efficiency and low cost. These features make it a better solution than the classical approach.

The first stage of the proposed UPS consists of an integrated battery charger, which was introduced in [1]. This topology uses a flyback converter in order to provide high power factor, battery charging, and high frequency isolation between both the main input (utility line) and the battery set to the load. This structure does the functions of battery charging and power factor correction by using just one magnetic structure, reducing costs and accomplishing high reliability and simplicity of the converter. The flyback converter can be operated either in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). If the converter works in DCM the control circuit is simpler. However, the use of the DCM flyback converter makes the proposed scheme just suitable for low power applications.

The second stage of the UPS is an inverter topology that features both boosting and inverting functions. This topology was previously introduced in [2]. The boost dc-ac converter, referred as *boost inverter*, features an excellent property; it naturally generates an ac output voltage that can be lower or larger than the dc input voltage, depending on the duty cycle [2]–[4]. This property is not found in the classical voltage source inverter, which produces an instantaneous ac output voltage always lower than the dc input voltage.

III. PFC-BATTERY CHARGER STAGE

The basic circuit of the PFC-battery charger is shown in Fig. 3. As it can be seen in this figure, the converter can accept two input powers: one through the ac line and the other through the battery set. The topology has three modes of operation [1]: normal mode, backup mode, and charging mode. The switch Q_1 controls the energy transfer in normal and charging operation mode, whereas Q_2 modulates the power transference

Manuscript received June 23, 1998; revised November 14, 2001. This paper was presented at the Power Electronics Specialists Conference, Saint Louis MO, 1997. Recommended by Associate Editor K. Smedley.

N. Vázquez is with the Electronics Engineering Department, Instituto Tecnológico de Celaya, Celaya, México (e-mail: nvazquez@itc.mx).

C. Aguilar and J. Arau are with the Electronics Engineering Department, CENIDET, Cuernavaca, México (e-mail: aguilar@cenidet.edu.mx; j.arau@ieee.org).

R. O. Cáceres is with the Engineering Electronics and Communication Department, Universidad de Los Andes, Mérida, Venezuela (e-mail: rcaceres@ing.ula.ve).

I. Barbi is with the Power Electronics Institute, Federal University of Santa Catarina, Florianópolis, SC, Brazil (e-mail: ivo@insep.ufsc.br).

J. Alvarez Gallegos is with the Electrical Engineering Department, CINVESTAV-IPN, México (e-mail: jalvarez@mail.cinvestav.mx).

Publisher Item Identifier S 0885-8993(02)04632-X.

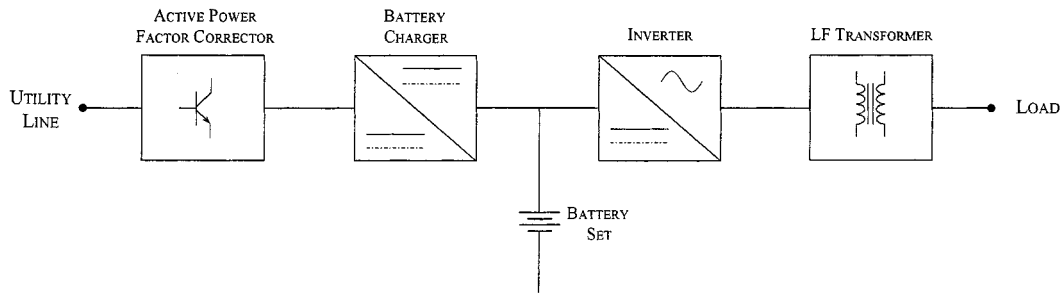
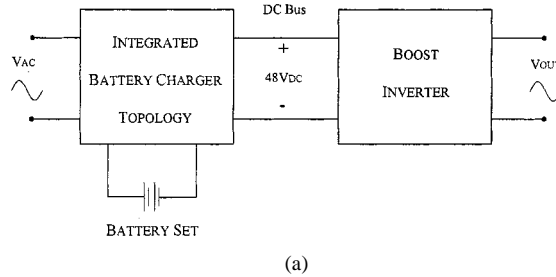
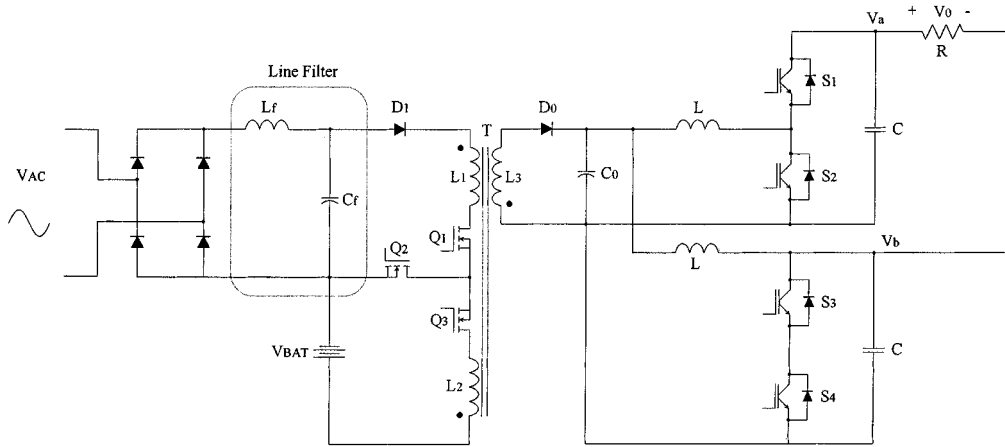


Fig. 1. Traditional uninterruptible power supply system with active PFC.



(a)



(b)

Fig. 2. Proposed uninterruptible power supply system: (a) block diagram and (b) circuit diagram.

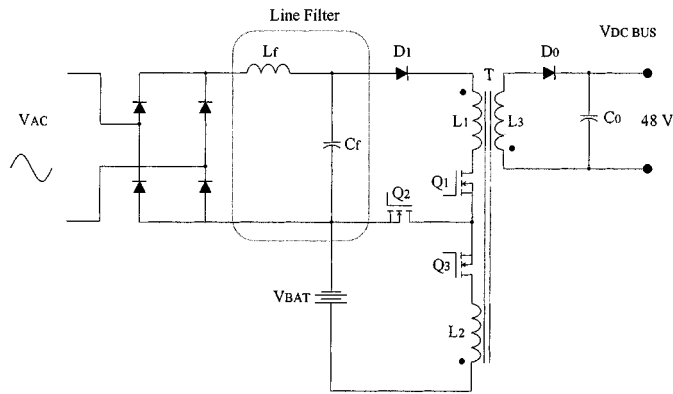


Fig. 3. Integrated battery charger topology as input stage of the proposed UPS.

when the converter operates in the backup operation mode. The main converter (V_{AC} , L_1 and Q_1) operates when the main utility line is working properly, whereas the backup converter (V_{BAT} , L_2 and Q_2) operates when the principal energy supply fails. The switch Q_3 selects between the normal operation

mode and the charging operation mode. At the same time, it controls the battery charging current. In addition, the switch Q_3 protects the battery from high current levels that overpass the specifications of the battery manufacturer.

The PFC-battery charger can operate either in DCM or CCM. If the converter is operated in CCM an extra loop, to control the converter input current, must be added. This complicates the control strategy and increases the cost; besides, another controller need be used for the backup operation mode. If the converter operates in DCM, only one loop is needed to control the output voltage, and the same controller can be used in normal and backup mode; based on this, the converter was tested in DCM.

In normal and charging operation modes, the equivalent circuit of the integrated battery charger topology is a flyback converter in DCM. Therefore, it behaves (in natural way) as a linear load to the utility line [5]. In the backup operation mode the equivalent circuit is a well-known dc-dc flyback converter. In this operation mode, as the battery voltage is low, the peak and average currents are higher than these ones in normal and

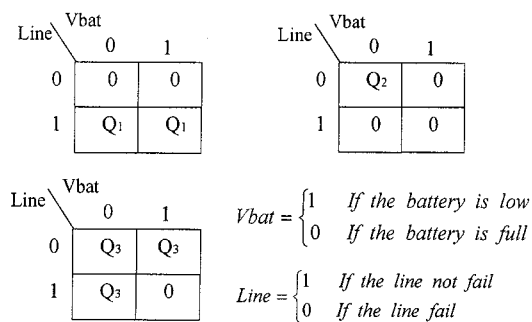


Fig. 4. Karnaugh maps.

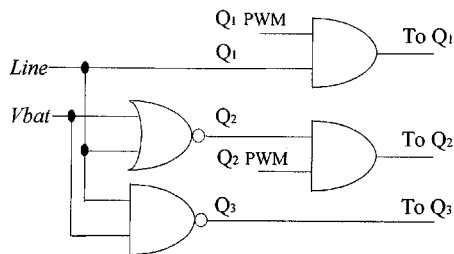


Fig. 5. Logic circuit that determines the operation modes of the PFC-battery charger.

charging operation mode. Therefore, we must be careful while selecting the battery voltage and the semiconductor devices.

The system includes a logic circuit that determines the gate signals for the PFC-battery charger power switches. This control circuit gives the Q_1 , Q_2 , and Q_3 gate signals according the battery and the utility line conditions. The logic circuit was obtained by using the Karnaugh maps shown in Fig. 4. The resultant circuit is shown in Fig. 5.

A. Some Experimental Results

An experimental prototype was designed and built. The specifications were as follow: output power = 200 W, input voltage = 120 V_{rms}, $V_{BAT} = 48$ V, and $V_{DCBUS} = 48$ V. The converter was implemented in DCM using mixed devices (MOSFET+IGBT) as power switches in order to increase the efficiency.

The experimental input voltage and current waveforms in normal operation mode are shown in Fig. 6. As can be seen, the voltage and current waveforms are in phase. Therefore, a close to one power factor and low THD were obtained.

The converter was tested in charging operation mode too. The experimental input voltage and current waveforms are shown in Fig. 7 during this operation mode. As we can see in this figure, the input current waveform has a dead time around crossing zero. This effect is due to the relatively high battery voltage [6], causing a reduction of the power factor and a higher THD than those ones in the normal operation mode. However, a higher V_{BAT} voltage means higher efficiency in the backup operation mode.

IV. BOOST INVERTER STAGE

The boost inverter achieves dc–ac conversion as follows: the power stage consists of two current bidirectional boost

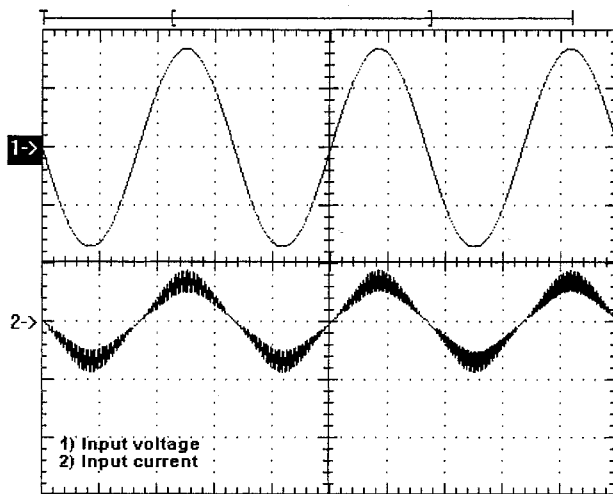


Fig. 6. Input voltage and current waveforms in normal operation mode (1- 100 V/div, 2- 4 A/div).

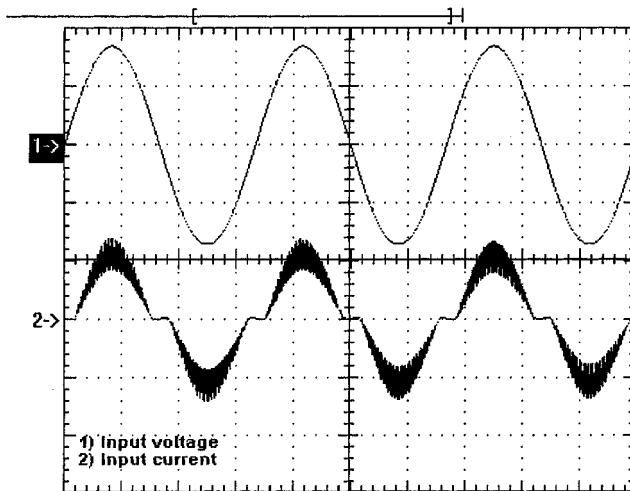


Fig. 7. Input voltage and current waveforms in charging operation mode (1- 100 V/div, 2- 4 A/div).

converters and the load is connected differentially across them (Fig. 8). These converters produce a dc-biased sinusoidal waveform; i.e., each converter produces a unipolar voltage. The modulation of each converter is 180° out of phase with respect to the other, which maximizes the voltage excursion over the load (Fig. 9) [3], [4].

For optimizing the boost inverter dynamics, while ensuring correct operation in any operative condition, the sliding mode controller is one of the most suitable approaches. The main advantage over the classical control schemes is its robustness for plant parameter variations and invariant steady state responses in the ideal case.

A. Analysis of the Boost Inverter

The converter is analyzed using the sliding mode control strategy. To do this the converter is modeled as two dc/dc boost converters, but one is considered as an ideal sinusoidal voltage source. On the other hand, there are two possible positions of the switch (−1 and 1). Taken into account these considerations,

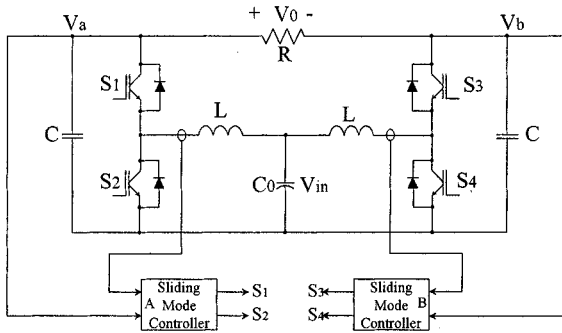


Fig. 8. Boost inverter with sliding mode control.

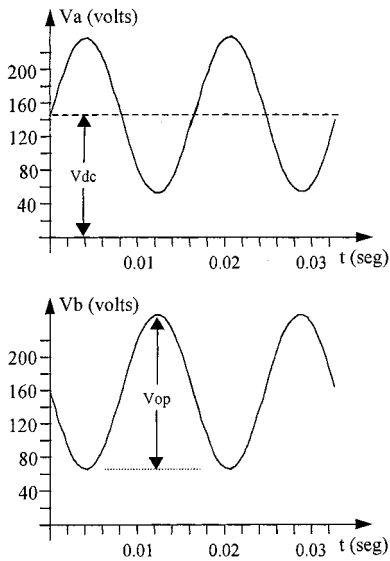


Fig. 9. Output voltage for each dc-dc converter.

the simplified circuit of the boost inverter is the shown in Fig. 10. The system equations in matrix form are:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -w_0/2 \\ w_0/2 & -w_1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 & w_0/2 \\ -w_0/2 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} u + \begin{bmatrix} b \\ c \end{bmatrix} \quad (1)$$

$$\dot{\mathbf{X}} = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{X}u + \mathbf{C} \quad (2)$$

where

$$x_1 = I_L \sqrt{L}, \quad x_2 = V_c \sqrt{C}, \quad w_0 = \frac{1}{\sqrt{LC}}, \quad w_1 = \frac{1}{RC},$$

$$b = \frac{V_{in}}{\sqrt{L}}, \quad c = \frac{V_b}{R\sqrt{C}}$$

Many papers have presented a guide for designing the sliding mode control [7]–[11]. In brief, the design steps could be summarized as follows:

- 1) propose the sliding surface;
- 2) verify the existence of a sliding mode
- 3) analyze the stability in the sliding surface.

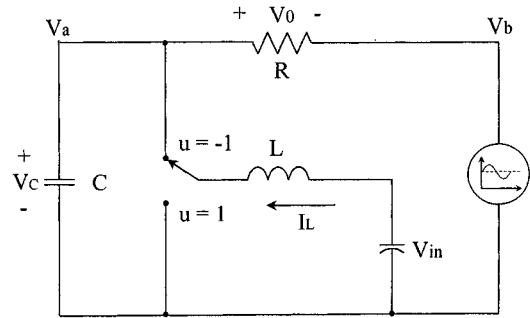


Fig. 10. Simplified circuit of the boost inverter.

i) The sliding surface.

The sliding surface proposed is a lineal combination of the state variables and the reference variables, that is

$$\sigma = \mathbf{S}\mathbf{X} - \mathbf{S}\mathbf{X}_r = \mathbf{S}\mathbf{e}\mathbf{X} \quad (3)$$

where

$$\mathbf{S} = [s_1 \quad s_2], \quad \mathbf{X} = \text{State variables},$$

$$\mathbf{X}_r = \text{Reference variables}, \quad \mathbf{e}\mathbf{X} = [ex_1 \quad ex_2]^T.$$

The control law proposed is

$$u = u_{eq} + u_N \quad (4)$$

where

$$u_{eq} = \text{Equivalent control}, \quad u_N = -\text{sgn} \sigma.$$

This control law is composed of two terms, the first one is only valid in the sliding surface (u_{eq}) and the other one assures the existence of a sliding mode.

ii) Existence of a sliding mode.

Existence of a sliding mode implies that the following condition is fulfilled [7]:

$$\sigma \dot{\sigma} < 0. \quad (5)$$

Solving for $\dot{\sigma}$

$$\dot{\sigma} = \mathbf{S} [\mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{X}u_{eq} + \mathbf{C} - \dot{\mathbf{X}}_r] + \mathbf{S}\mathbf{B}\mathbf{X}u_N. \quad (6)$$

Therefore

$$\sigma \dot{\sigma} = \mathbf{S}\mathbf{B}\mathbf{X}[-\sigma \text{sgn} \sigma] < 0. \quad (7)$$

This equation can be obtained by using the equivalent control, that is

$$u_{eq} = -[\mathbf{S}\mathbf{B}\mathbf{X}]^{-1}[\mathbf{S}\mathbf{A}\mathbf{X} + \mathbf{S}\mathbf{C} - \dot{\mathbf{X}}_r]. \quad (8)$$

In order to guarantee the existence conditions of a sliding mode, the following inequality must be fulfilled:

$$\mathbf{S}\mathbf{B}\mathbf{X} > 0 \quad (9)$$

Or

$$s_1 x_2 - s_2 x_1 > 0. \quad (10)$$

In order to assure the existence conditions, s_1 must be positive (due to x_2 is always positive) and greater than the absolute value of s_2 .

iii) Stability analysis in the sliding surface.

A tool developed to describe the movement in the sliding surface is the equivalent control [12]. The equivalent control is applied when $\sigma = 0$, hence $\dot{\sigma} = 0$. These conditions imply that the system is in the sliding surface.

The equivalent control (u_{eq}) is given by the (8) [12]. In this, the condition $\mathbf{SBX} \neq 0$ must be satisfied to avoid singularities in the equivalent control. The equivalent control must be substituted in the model of the system and the stability analysis must be made under this condition. For the system, we are dealing with the stability analysis, which is complicated due to the non-linear systems that result. Some methodologies could be applied (Liapunov-like methods, for instance) but that analysis is beyond the purpose of the present work.

B. Design Example

The design of the boost inverter is made considering that the switching frequency (f_s) is higher than 60 Hz and a resistive load is used. The parameters used are $P_o = 200$ W, $f_{s_{max}} = 30$ kHz, $V_{in} = 48$ V, $V_o = 120$ V_{rms}. The implementation is based on the maximum ripple desired in the inductor current and capacitor voltage.

First, the dc component of the capacitor voltage (V_{dc}) is calculated [4]

$$V_{dc} \geq \frac{V_{op}}{2} + V_{in} \quad (11)$$

where: $V_{op} =$ Peak output voltage ≈ 170 V.

Using (11), V_{dc} results 133 V. In order to avoid a “trimmed” output voltage, V_{dc} is chosen 150 V. The maximum capacitor voltage and inductor current is determined by [4]

$$V_{c_{max}} = V_{dc} + \frac{V_{op}}{2} \quad (12)$$

$$I_{L_{max}} = \frac{2D_{max} - G'_m(1 - D_{max})}{(1 - D_{max})^2} \cdot \frac{V_{in}}{R} \quad (13)$$

where

$$D_{max} = 1 - \frac{V_{in}}{V_{dc} + \frac{V_{op}}{2}}, \quad G'_m = \frac{2(V_{dc} - V_{in})}{V_{in}}$$

Solving, $D_{max} \approx 0.8$, $V_{c_{max}} = 235$ V, and $I_{L_{max}} = 12.5$ A. The inductance and capacitance are calculated with a 20% and 1.5% of ripple, respectively

$$L = \frac{t_{on}}{0.2I_{L_{max}}} V_{in} \quad (14)$$

$$C = \frac{t_{on}}{0.015V_{c_{max}}} I_{op} \quad (15)$$

where: $I_{op} =$ Peak output current ≈ 2.35 A.

As the switching boulder technique used is maintaining the turn on time constant [13], t_{on} is calculated with

$$t_{on} = \frac{D_{max}}{f_{s_{max}}} \quad (16)$$

Then, $t_{on} \approx 28$ μ S. Substituting (16) in (14) and (15), the inductance and capacitance are $L \approx 530$ μ H and $C \approx 22$ μ F. To calculate the controller parameters is necessary to found the boundary of the existence of the sliding mode, determined by

$$s_1 = \frac{s_2 x_{1P}}{x_{2P}} \quad (17)$$

where: $x_{1P} = I_{L_{max}} \sqrt{L}$, $x_{2P} = V_{c_{max}} \sqrt{C}$.

Using (17) and chosen s_2 equal to one, it gets $s_1 \approx 0.26$; in order to assure the sliding mode, the parameter s_1 must be higher than 0.26. Therefore, s_1 equal one is chosen.

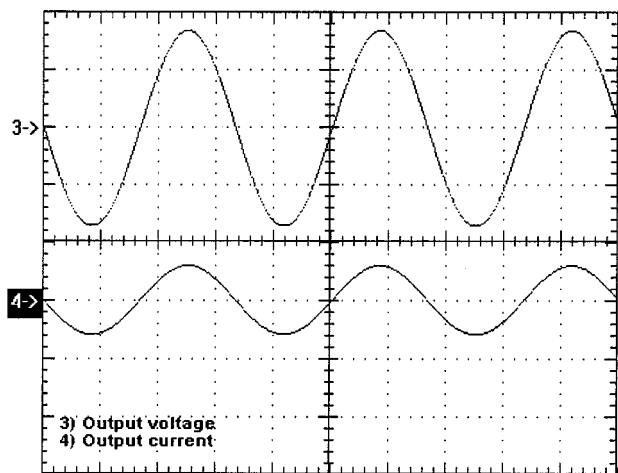


Fig. 11. Output voltage and current for resistive load operation (3–100 V/div, 4–4 A/div).

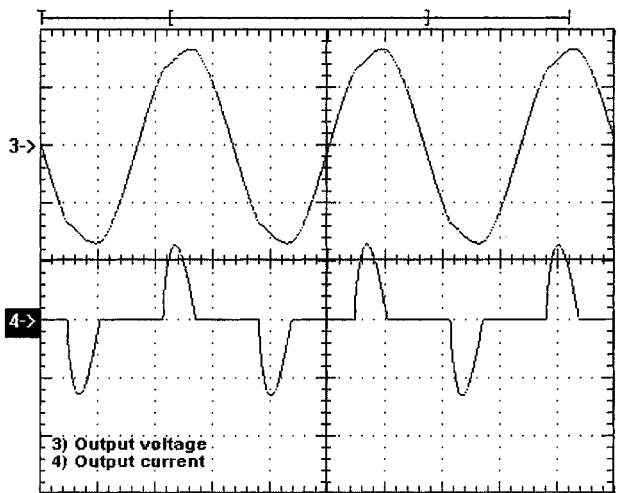


Fig. 12. Output voltage and current waveforms for nonlinear load operation (3–100 V/div, 4–4 A/div).

C. Some Experimental Results

An experimental prototype was designed and built. The specifications were $P_o = 200$ W, $V_{in} = 48$ V, and $V_o = 120$ V_{rms}. The experimental output voltage and current waveforms under resistive load are shown in Fig. 11. As we can see, the voltage has negligible distortion. The experimental output voltage and current waveforms under nonlinear load are shown in Fig. 12. As we can see, the voltage has a small distortion.

V. OVERALL SYSTEM PERFORMANCE

The complete system was tested under different operation conditions:

- 1) the performance of the converter in normal and charging conditions is addressed;
- 2) the performance under load variations;
- 3) the operation under nonlinear load;
- 4) the operation when the utility line fails.

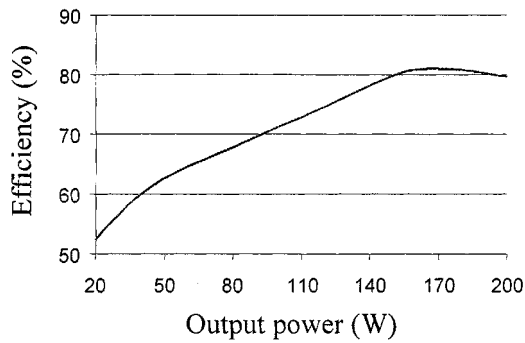


Fig. 13. Efficiency of the complete system.

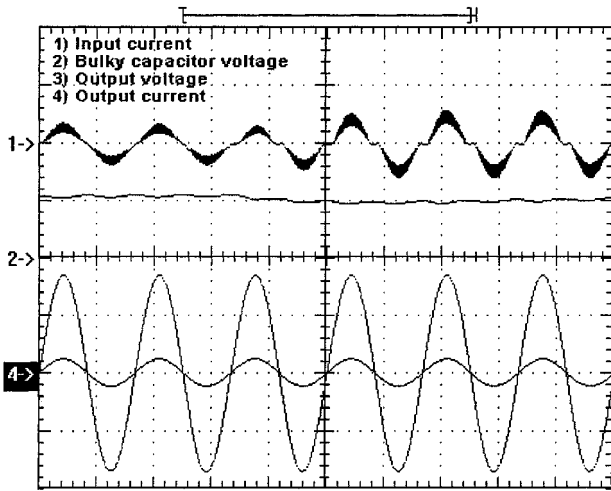


Fig. 14. System evolution when changes from normal to charging mode (1–5 A/div, 2–50 V/div, 3–100 V/div, 4–5 A/div).

A. Normal and Charging Operation Mode

The efficiency in normal mode is shown in Fig. 13. The maximum input current THD obtained was 6.5%, the maximum output voltage THD was 1.5%, and the PF was 0.98.

Fig. 14 shows the system response when the PFC-battery charger changes from normal to charging operation mode. This figure shows the input current, the bulky capacitor voltage (output voltage of the battery charger), and the output voltage and current waveforms. As can be observed, the input current increases because of the battery is being charged. In charging mode the maximum input current THD was 21%, and the PF was 0.91.

B. Load Variation

In order to verify the fastness of the system a load variation was made. The load variation was from 100 W to 200 W and viceversa. The input current, bulky capacitor voltage (output voltage of the battery charger), and output voltage and current waveforms are shown in Fig. 15. Fast response at the output voltage is obtained due to the excellent performance of the sliding mode control. As can be seen, the bulky capacitor voltage falls lightly; despite this, the output voltage keeps constant. A relative slow response is observed at the input current, this is because a reduced bandwidth is needed to correct the power factor.

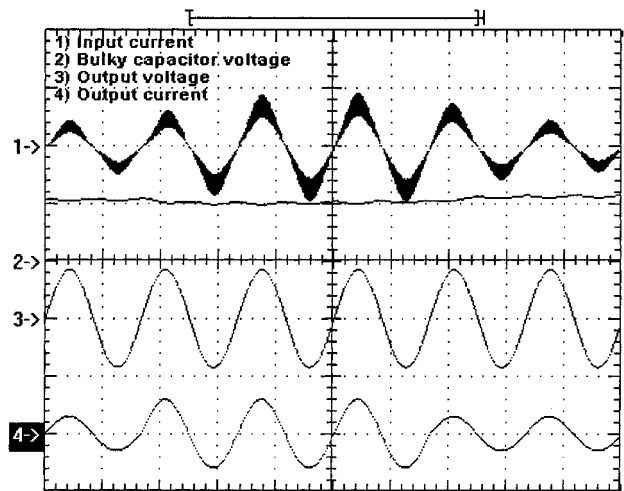


Fig. 15. System evolution under linear load variation (1–4 A/div, 2–50 V/div, 3–200 V/div, 4–4 A/div).

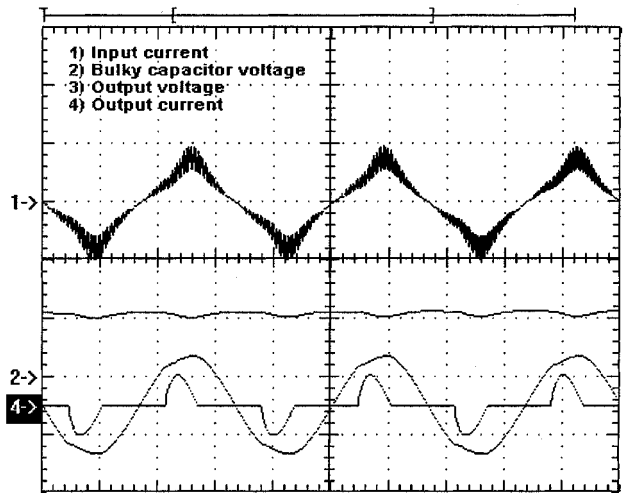


Fig. 16. System evolution under non linear load. (1–2 A/div, 2–50 V/div, 3–200 V/div, 4–5 A/div).

C. Nonlinear Load

The complete system was also tested under nonlinear load conditions. The input current, bulky capacitor voltage, and output voltage and current waveforms are shown in Fig. 16. A small distortion appears at the output voltage when the current increases suddenly. The THD of the output voltage is 4.5%. Also, a small distortion is “reflected” to the input current, this is because the bulky capacitor is discharged when the load demands current. The THD of the input current under this condition is 20%. The THD could be reduced by increasing the bulk capacitor value, or reducing the bandwidth of the PFC-battery charger control loop.

D. Outage Test

The system was tested under failing and reestablishing the utility line. Fig. 17 shows the input current, outage detector, and the output voltage and current waveforms when the utility line fails. At the outage time, the PFC-battery charger changes from normal to backup operation immediately. As can be seen, the output voltage keeps regulated without interruptions. Fig. 18

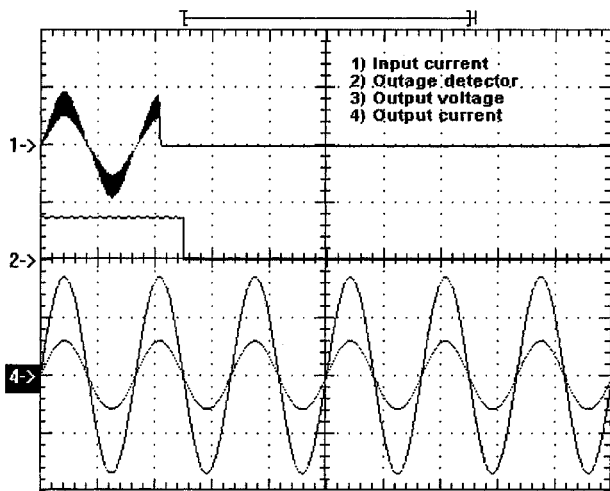


Fig. 17. System evolution under an outage test (1–4 A/div, 2–20 V/div, 3–100 V/div, 4–4 A/div).

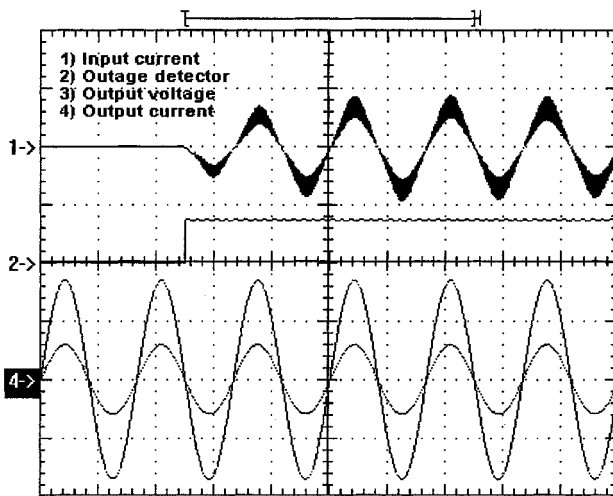


Fig. 18. System evolution when the utility line is reestablished (1–4 A/div, 2–20 V/div, 3–100 V/div, 4–4 A/div).

shows the system response when the outage ends, that is, when the utility line is reestablished. As can be seen, the output voltage keeps regulated without transient by the transition in the input voltage. The input current, outage detector, and the output voltage and current waveforms are shown in Fig. 18 when the utility line is reestablished.

VI. CONCLUSION

At present days, it is very important to achieve high efficiency, low cost, and high reliability in UPS designs, and at the same time to fulfill the power quality standards (concerning the characteristics of power factor and total harmonic distortion on the input current). This paper presents a novel approach in order to meet these objectives. The design is based on the reduction of the power conversion stages in both the battery charger and the inverter stages.

The novel approach is the result of a combination of two converters previously proposed by the authors. For the PFC and battery charger section of the UPS an integrated topology based on the flyback converter in DCM operation is proposed [6], which

offers a simple way for controlling battery charging as well as the PFC characteristics in the converter.

On the other hand, for the inverter stage, a recently proposed inverter is used [2]. The inverter stage is based on dc-dc boost converters obtaining a topology that features inverting and boosting functions at the same. In order to get a good dynamic response a sliding mode control is used to improve these characteristics.

Besides the high efficiency obtained in the proposed UPS, an additional benefit to the previously mentioned approaches has been obtained: a good dynamic response of the output voltage and high power factor at the input.

REFERENCES

- [1] C. Aguilar, F. Canales, J. Arau, J. Sebastián, and J. Uceda, "An integrated battery charger/discharger with power factor correction," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 597–603, Oct. 1997.
- [2] R. Cáceres and I. Barbi, "A boost dc-acconverter: Operation, analysis, control and experimentation," in *Proc. Int. Conf. Ind. Electron., Contr. Instrum.—IECON'95*, Orlando, FL, Nov. 1995, pp. 546–551.
- [3] —, "Sliding mode controller for the boost inverter," *Proc. IEEE Int. Power Electron. Congr.—CIEP'96 Conf.*, pp. 247–252, Oct. 1996.
- [4] N. Vázquez, "New topology of inverter based on the dc/dc boost converter," M.Sc. thesis, Centro Nacional de Investigación y Desarrollo Tecnológico (CENIDET), Cuernavaca, México, Nov. 1997, in Spanish.
- [5] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter," *Proc. IEEE Appl. Power Electron. Conf.—APEC'90 Conf.*, pp. 792–801, Mar. 1990.
- [6] C. Aguilar, "Analysis of a novel scheme of an integrated battery charger/discharger with high power factor," M.Sc. thesis, Centro Nacional de Investigación y Desarrollo Tecnológico (CENIDET), Cuernavaca, México, Feb. 1995, in Spanish.
- [7] R. A. DeCarlo, S. Zak, and G. P. Matthews, "Variable structure control of nonlinear multivariable systems: A tutorial," *Proc. IEEE*, vol. 76, pp. 212–232, Mar. 1988.
- [8] J. Y. Hung, W. Gao, and J. C. Hung, "Variable structure control: A survey," *IEEE Trans. Ind. Electron.*, vol. 40, pp. 2–18, Feb. 1993.
- [9] H. Sira-Ramírez and M. Ilic, "A geometric approach to the feedback control of switch mode dc-to-dc power supplies," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1291–1298, Oct. 1988.
- [10] P. Mattavelli, L. Rossetto, and G. Spiazzi, "General purpose sliding mode controller for dc/dc converter applications," *Proc. IEEE Power Electron. Spec. Conf.—PESC'93 Conf.*, pp. 609–615, June 1993.
- [11] M. Carpita and M. Marchesoni, "Experimental study of a power conditioning using sliding mode control," *IEEE Trans. Power Electron.*, vol. 11, pp. 731–742, Sept. 1996.
- [12] V. I. Utkin, *Sliding Modes and Their Application in Variable Structure Systems*. Moscow, Russia: MIR, 1974.
- [13] B. J. Cardoso, A. F. Moreira, B. R. Menezes, and P. C. Cortizo, "Analysis of switching frequency reduction methods applied to sliding mode controlled dc-dc converters," *Proc. IEEE Appl. Power Electron. Conf. Expo.—APEC'92 Conf.*, pp. 403–410, Feb. 1992.



Nimrod Vázquez (S'98) was born in México DF, México, in 1973. He received the B.S. degree in electronics engineering from the Instituto Tecnológico de Celaya, México, in 1994, the M.Sc. degree in electronics engineering from the National Center for Research and Technological Development (CENIDET), México, in 1997 where he is currently pursuing the Dr.Eng. degree.

From 1994 to 1995, he was in the Research Technological Teaching Program, Electrical Research Institute (IIE), Cuernavaca, México. In 1998, he joined the Electronics-Engineering Department, Instituto Tecnológico de Celaya. His fields of interest include dc/ac converters, power factor correction, and nonlinear control techniques, in which he has published more than 18 papers in conferences.

Mr. Vázquez received the Medal of the Mexico Daily as the Best Mexican Student in 1994, the Third Place Prize in the National Contest of Basic Sciences in 1994, and the First Place Prize in the National Contest of Creativity in 1997.



Carlos Aguilar (M'94) was born in Tres Valles, Veracruz, México, in 1970. He received the B.S. degree in electromechanical engineering from the Instituto Tecnológico de Tuxtepec, México, in 1992 and the M.Sc. and Ph.D. degrees in electronics engineering from the National Center for Research and Technological Development (CENIDET), México, in 1995 and 1998, respectively.

His research interest include power-factor correction, dc power supplies, and distributed power supply systems.



Jaime Arau (M'92–SM'97) was born in Veracruz, Mexico, in 1960. He received the B.Sc. degree in electronic engineering from the Instituto Tecnológico de Minatitlán, Minatitlán, Mexico, in 1982 and the Ph.D. degree in electrical engineering from the Universidad Politécnica de Madrid, Madrid, Spain, in 1991.

From 1982 to 1994, he was a Researcher at the Electrical Research Institute (IIE), Cuernavaca, Mexico, where he conducted the Power Electronics Group from 1992 to 1994. He is currently a Professor

at the Electronics Department and Vice-Director for Academic and Research Affairs, National Center for Research and Technological Development (CENIDET), Cuernavaca, Mexico, where he teaches and conducts research in the area of power electronics. His fields of interest are high-power-factor rectifiers, electronic ballasts, active power filters, and converters modeling, in which he have published more than 70 papers in international journal and conferences.

Dr. Arau received the IEEE Third Millennium Medal and is a member of the Mexican Academy of Sciences. He was the Founding President of the IEEE Morelos Section (Mexico) Power Electronics Chapter, was the PELS Region 9 Liaison (1996–1997), and is currently serving as an AdCom Member and Chapters Coordinator. He will serve as the General Chairman of the IEEE Power Electronics Specialist Conference-PESC'03, Acapulco, Mexico, 2003.



Ramón O. Cáceres (M'97) was born in San Cristóbal, Táchira, Venezuela, in 1959. He received the B.S. degree in electrical engineering from the Universidad de los Andes, Mérida, Venezuela, in 1983 and the M.S. and Ph.D. degrees from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1993 and 1997, respectively.

In 1985, he joined the Department of Electronics, Universidad de los Andes, where he is currently a Professor and Member of the Power Electronics Research Group. His research interest includes dc/dc

and dc/ac converters, PF correction, and soft-switching techniques.



Ivo Barbi (M'78–SM'90) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Power Electronics Institute (INEP), Federal University of Santa Catarina. He is a Professor with the Power Electronics Institute, Federal University of

Santa Catarina.

Dr. Barbi has been an Associate Editor in the Power Converters Area of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since January 1992.



Jaime Alvarez Gallegos (M'89–SM'97) was born in Tampico, Mexico. In 1973, he received the B.S. degree in electronics engineering from the National Polytechnic Institute of Mexico (IPN) and the M.Sc. and Ph.D. degrees in electrical engineering from the Center for Research and Advanced Studies, CINVESTAV, Mexico, in 1974 and 1978, respectively.

He has been head of the Automatic Control Section, CINVESTAV, from 1983 to 1985, head of the Department of Electrical Engineering, CINVESTAV, 1992 to 1996, and Director of the School of Interdisciplinary Engineering and Advanced Technologies of the IPN, 1997 to 2000.

He also held the position of Visiting Professor at the Imperial College of Science and Technology, London, U.K., 1985 to 1986. Since 1976, he has been a Professor in the Department of Electrical Engineering, CINVESTAV. He is also a National Researcher of the System of National Researchers. He has been lecturer in more than 20 different courses. He has published around 120 scientific papers in international journals and conference proceedings and coordinated 11 projects in applied research.

Dr. Gallegos is a member of the Mexican Academy of Sciences and the Mexican Academy of Engineering.