

Zero-Voltage Switching for the Neutral-Point-Clamped (NPC) Inverter

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Abstract—This paper proposes a transformer-assisted pulsewidth-modulation zero-voltage-switching neutral-point-clamped (NPC) inverter. With the assistance of a transformer-assisted small-rating lossless auxiliary circuit, the main switches work with zero-voltage switching without suffering from any voltage/current spikes, under simple explicit control. The technique allows for higher operating frequency and better device utilization of the NPC inverter. Operation, analysis, design, as well as testing results from a 7-kW prototype are presented in detail.

Index Terms—Neutral-point-clamped inverter, zero-current switching, zero-voltage switching.

I. INTRODUCTION

THE neutral-point-clamped (NPC) inverter [1] has been playing a growing role in the past decade in drive [2], [4] and power system applications [3], due to the expanded capacity with the existing devices without the problematic series association, as well as the reduced output harmonics. To limit the dv/dt and di/dt rate of change of the switching device, different snubber schemes utilizing either RCD snubbers [4] or low-loss snubbers [5], [6] have been developed, where the switching frequency has been substantially limited due to the significant snubber loss. Regenerative snubbers avoid the loss at the expense of the considerable hardware complexity [7], [8], which may even include baby snubbers for the recovery choppers [9]. Moreover, snubbers, either dissipative or regenerative, suffer from such other problems as voltage/current spikes, series inductor loss, as well as the adverse effects from the snubbing diodes [10], etc.

Several previous publications have resorted to soft-switching techniques for snubbing of the NPC inverter. Besides the early thyristor three-state inverter [11] which actually works with zero-current switching, zero-voltage switching schemes realized with resonant dc link [12] and auxiliary resonant commutated-pole-inverter (ARCPI) [13] have also been investigated [14], [15]. In particular, the ARCPI NPC inverter [15], as shown in Fig. 1 seems a more promising scheme for high-power applications due to the small-power auxiliary circuit and full pulsewidth-modulation (PWM) operation capability. However, the scheme requires complicated current monitoring and controlling to ensure zero-voltage switching

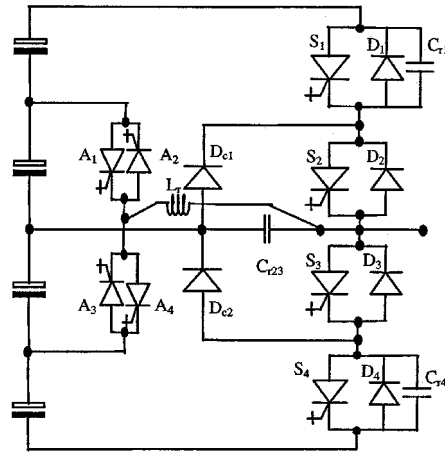


Fig. 1. Configuration of the ARCPI NPC inverter proposed in [15], based on the two-level origin [13].

[13], especially when possible fluctuation of the dc-link capacitor center-tap potentials are taken into account [16]. Protection of the auxiliary devices (A_1 – A_4) from voltage spikes during their reverse recoveries constitutes the other difficulty of the circuit [17]. Moreover, the auxiliary devices in the circuit are subject to 1.5 times the main devices blocking voltage, significantly raising the cost for the auxiliary circuit.

As shown in Fig. 2, this paper proposes an alternative zero-voltage-switching scheme for the NPC inverter, based on the two-level origin [18]. By setting the transformer ratio k ($k = N_2/N_{11} = N_2/N_{12}$) to less than 1/4 according to the potential resonant loop losses, the proposal requires no additional monitoring or controlling circuit for ensuring zero-voltage operation. Moreover, as the auxiliary devices are all clamped to the dc rails by the NPC configuration, an overvoltage protecting circuit is no longer necessary. Except for D_{11} and D_{12} , all the auxiliary devices block the same voltage as the main devices, rendering the circuit more practically interesting. It is worth mentioning that the D_{11}/D_{12} blocking voltage can be halved by using a full-bridge structure [18]. The number of diodes, however, is also doubled. Operation, analysis, design, and testing of the circuit will be presented in this paper.

II. CIRCUIT OPERATION

Neglecting the effects from the second-order circuit parasitics as stray inductances and capacitances, etc., the whole circuit can be decoupled into two independent zero-voltage-switching poles, as shown in Fig. 3(a) and (b). The stability of the dc-link neutral potential has been addressed extensively in the literature

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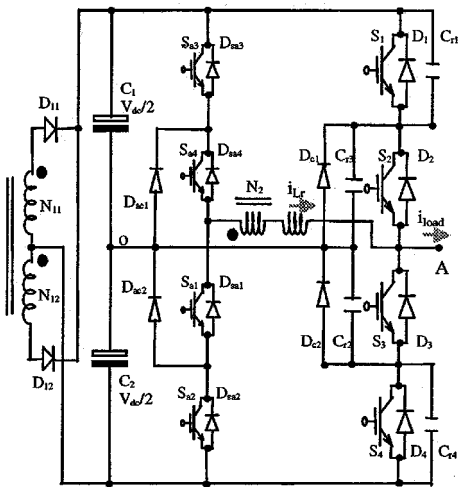


Fig. 2. Configuration of the proposed transformer-assisted PWM zero-voltage-switching pole NPC inverter, based on the two-level origin [18] ($k = N_2/N_{11} = N_2/N_{12} < 1/4$).

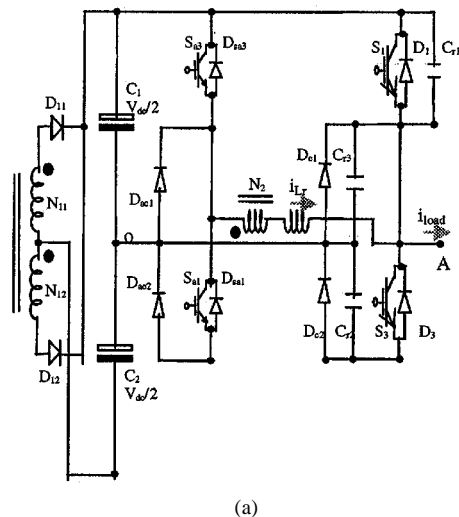
[19]. It will be assumed constant and will not be dealt with further for the sole purpose of this paper.

For the first pole, as shown in Fig. 3(a), the output can be switched between the plus rail and the zero rail by gating S_1 and S_3 alternatively, while S_2 is always ON and S_4 is always OFF in the main circuit, and S_{a4} is always ON and S_{a2} is always OFF in the auxiliary circuit. As a result, for the main circuit, D_{c1} forms the freewheeling path of the down-arm, and S_3 in series with D_{c2} forms the forward path of the down-arm. In the meanwhile, C_{r2} always sees zero voltage, whereas C_{r3} serves as the snubbing capacitance for the down-arm. Moreover, for the auxiliary circuit, D_{ac1} forms the freewheeling path of the down-arm, and S_{a1} in series with D_{ac2} forms the forward path of the down-arm.

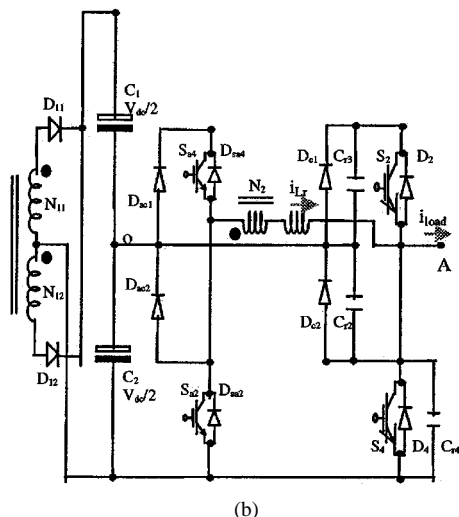
For the second pole, as shown in Fig. 3(b), the output can be switched between the zero rail and the minus rail by gating S_2 and S_4 alternatively, while S_3 is always ON and S_1 is always OFF in the main circuit, and S_{a1} is always ON and S_{a3} is always OFF in the auxiliary circuit. Similar to the first pole, in the main circuit, D_{c2} forms the freewheeling path of the up-arm and S_2 in series with D_{c1} forms the forward path of the up-arm. C_{r3} always sees zero voltage whereas C_{r2} serves as the snubbing capacitance for the up-arm. Also, in the auxiliary circuit, D_{ac2} forms the freewheeling path and S_{a4} in series with D_{ac1} forms the forward path of the up-arm.

Evidently, both of the decoupled circuits work as a transformer-assisted PWM zero-voltage-switching pole inverter [18]. In Fig. 3(a), auxiliary switches S_{a1} and S_{a3} assist the commutations of S_1 and S_3 , respectively, in the first zero-voltage-switching pole. On the other hand, in Fig. 3(b), auxiliary switches S_{a2} and S_{a4} assist the commutations of S_2 and S_4 , respectively, in the second zero-voltage-switching pole.

As operation of one pole is identical to the other, only the operation of the first pole will be described. Assume that for each snubbing capacitance, a zero-voltage detecting circuit is installed across it for releasing the gating signal of its corresponding main device ($C_{r1} - S_1; C_{r2} - S_2; C_{r3} - S_3; C_{r4} - S_4$)



(a)



(b)

Fig. 3. Decoupling of the transformer-assisted PWM zero-voltage-switching pole NPC inverter into two independent poles. (a) First zero-voltage-switching pole of the transformer-assisted PWM zero-voltage-switching NPC inverter. S_2 is always ON and S_4 is always OFF in the main circuit. S_{a4} is always ON and S_{a2} is always OFF in the auxiliary circuit. (b) Second zero-voltage-switching pole of the transformer-assisted PWM zero-voltage-switching NPC inverter. S_3 is always ON and S_1 is always OFF in the main circuit. S_{a1} is always ON and S_{a3} is always OFF in the auxiliary circuit.

[18]. Assume further that the transformer ratio k is set less than $1/4$ which ensures the pole voltage swinging to the rail level during the commutation resonance with the presence of commutation loop losses [18]. Referring to Fig. 4 for the commutation step diagrams and Fig. 5 for the predicted commutation waveforms, the commutations between $S_1(D_1)$ – S_3 during a switching cycle under negative load current condition will proceed in the steps described as follows.

- Step 1) (t_0-t_1): Circuit steady state. Freewheeling diodes D_2 and D_1 carry the load current. Circuit output is connected to the plus rail.
- Step 2) (t_1-t_2): Turn off S_1 and turn on S_{a1} simultaneously at t_1 , leading to conduction of the auxiliary diode D_{12} . A voltage source valued at kV_{dc} is induced on N_2 . Currents in D_1 and D_2 start decreasing.
- Step 3) (t_2-t_3): D_1 and D_2 becomes blocking at t_2 . C_{r1} is then charged and C_{r3} is discharged.

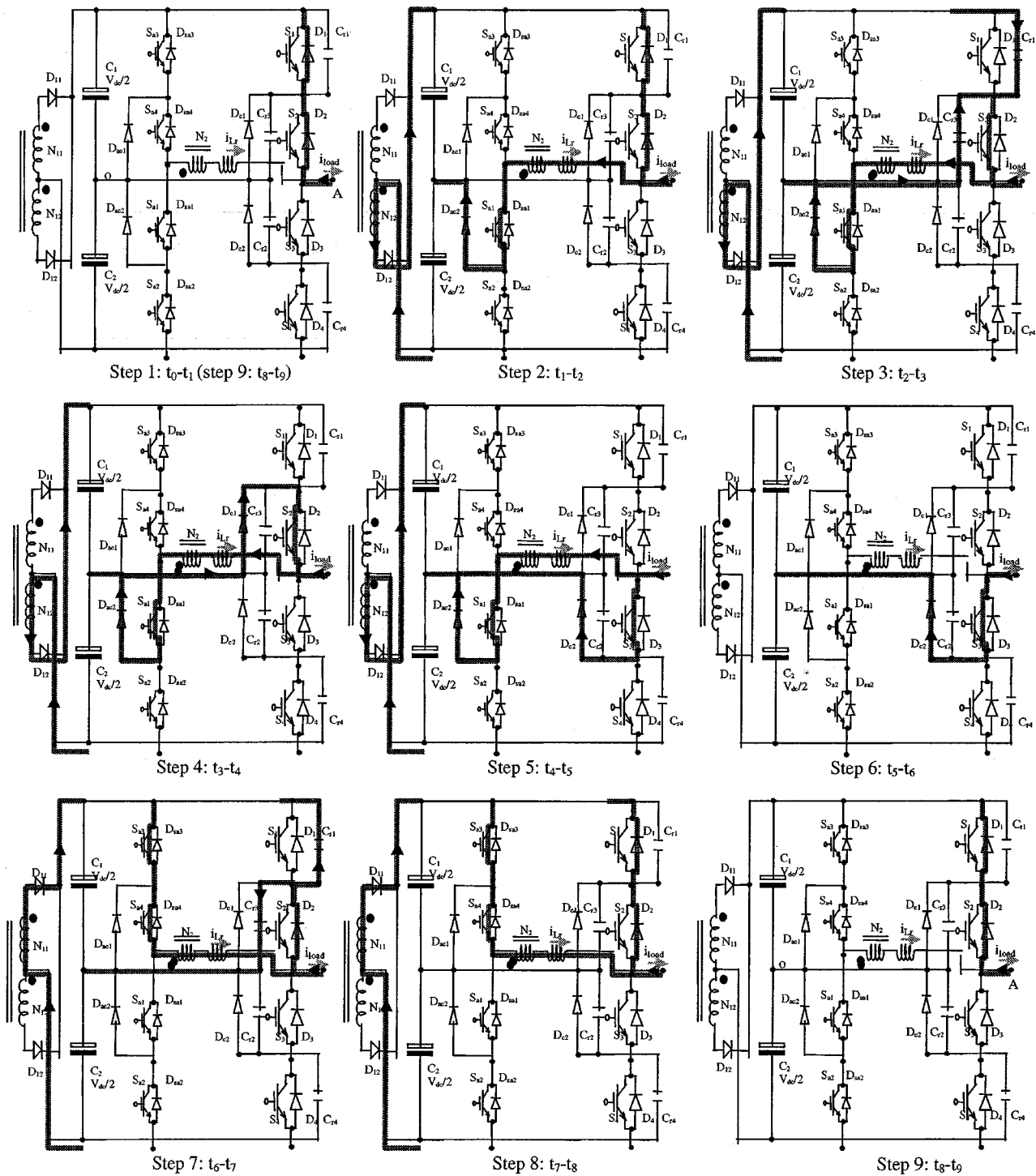


Fig. 4. Step diagrams for the commutations between S_1 – S_3 when the load current is negative (k is the transformer ratio, $k = N_2/N_{11} = N_2/N_{12} < 1/4$).

- Step 4) (t_3 – t_4): C_{r1} voltage rises to $V_{dc}/2$ at t_3 . Currents transfer from C_{r1} and C_{r3} to D_{c1} instantly. S_3 gating signal is then released by the zero-voltage detecting circuit installed across C_{r3} .
- Step 5) (t_4 – t_5): Resonant inductor current i_{Lr} decreases to the load current level i_{load} at t_4 . D_{c1} becomes blocking and S_3 starts conduction.
- Step 6) (t_5 – t_6): Resonant inductor current i_{Lr} and the auxiliary diode current in D_{12} decreases to zero at t_5 .

S_{a1} gating signal can be withdrawn. Circuit reaches another steady state. The output is connected to the zero rail. S_3 and D_{c2} carry the load current.

- Step 7) (t_6 – t_7): Turn off S_3 and turn on S_{a3} at t_6 , leading to conduction of the auxiliary diode D_{11} . An induced voltage source of kV_{dc} appears on N_2 . C_{r3} is charged and C_{r1} is discharged.
- Step 8) (t_7 – t_8): C_{r1} voltage declines to zero at t_7 . Currents in C_{r1} and C_{r3} transfer to D_1 instantly. S_1 gating

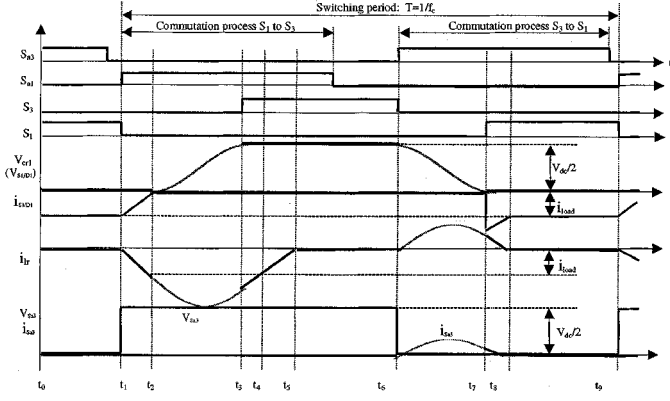


Fig. 5. Predicted theoretical waveforms for the commutations between S_1 – S_3 in the first zero-voltage-switching pole with negative load current during a switching cycle.

signal is released by the zero-voltage detecting circuit installed across it.

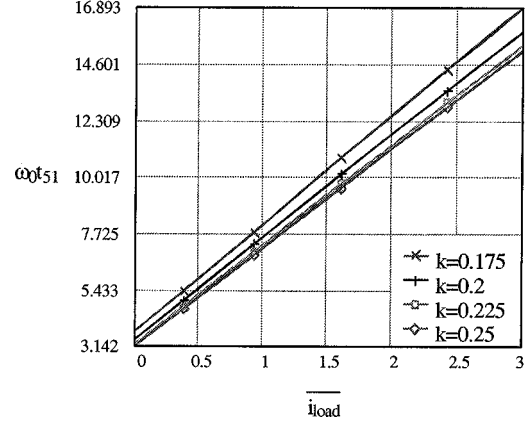
Step 9) (t_8 – t_9): Currents in the resonant inductor L_r and the auxiliary diode D_{11} extinct at t_8 . S_{a3} gating signal can be withdrawn. Circuit returns to the original state. D_2 and D_1 carry the load current. Circuit output is connected to the plus rail.

In practice, due to magnetization of the transformer, following each commutation, a residual current will flow in the auxiliary switch and the transformer secondary, when the resonant current in the auxiliary diode and the transformer primary reaches zero. This residual current will not be reset until the turn-off of the auxiliary switch, which must be well taken into account during transformer designing, so that the residual current will be minimized.

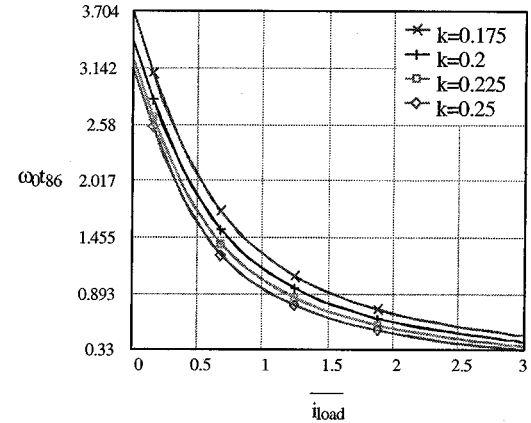
Note that the inner switch S_3 may not work exactly at zero-voltage switching in practice when the parasitic inductances and capacitances of the circuit are taken into account. Assume a parasitic inductance with the neutral rail and a negative load current flowing through S_3 and D_{c2} connecting the output to the neutral rail. Now, to transfer the load current from S_3 and D_{c2} to D_2 and D_1 , the neutral rail current will decrease leading to discharging of the resonant capacitor C_{r4} via D_{c2} . Upon reaching the steady state (D_2 and D_1 conducting), both C_{r2} and C_{r4} will be charged by C_2 via the parasitic inductance of the neutral rail. Consequently, voltage across C_{r2} will not be zero. Thus for the next commutation, the turn-on of S_3 will see the discharging of C_{r2} and will not exactly be zero-voltage switching as a result.

Analogously, inner switch S_2 will see the same problem in the second pole when load current is positive.

This problem is essentially resulted from the topological drawback of the NPC inverter, i.e., the inner two switches of a NPC leg are actually not directly clamped as in the two-level inverter. It is S_3 in series with D_{c2} that is clamped to C_1 , rather than S_3 itself. In the same sense, it is S_2 in series with D_{c1} that is clamped to C_2 , rather than S_2 itself. Therefore, when S_3 and S_4 are both OFF, S_3 can block higher voltage than S_4 and D_{c2} can see some voltage rather than zero, or, alternatively, when S_1 and S_2 are both OFF, S_2 can block higher voltage than S_1 and D_{c1} can see some voltage rather than zero.



(a)



(b)

Fig. 6. Variations of commutation durations t_{51} and t_{86} with load current and transformer ratio; mathematical expressions for t_{51} and t_{86} are given in Table I. (a) Diode-to-switch commutation. (b) Switch-to-diode commutation.

This problem can be resolved by paralleling to each clamping diode (D_{c1}/D_{c2}) a small rating switch so that a direct clamping path for the corresponding main switch (S_2/S_3) is established. In practice, the problem can be well mitigated by fine low-inductance bus-bar designing.

III. CIRCUIT ANALYSIS AND DESIGNING

Since each pole works in the same way as the two-level transformer-assisted PWM zero-voltage-switching pole inverter, the characteristics of the two-level transformer assisted PWM zero-voltage-switching pole inverter applies also in the present circuit. Under the following assumptions, the commutation duration, the resonant inductor peak current, the resonant inductor rms current (averaged over the switching cycle) and the resonant capacitor rms current (averaged over the switching cycle) in relation to load current, transformer ratio, and switching cycle are shown in Figs. 6–10, respectively. Details of the mathematical expressions [18] have been included in Tables II–V.

- Snubbing capacitance $C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_r$, resonant frequency $\omega_0 = 1/\sqrt{2C_r L_r}$, resonant impedance $Z_o = \sqrt{L_r/2C_r}$, and switching cycle T . Unit current $\bar{i} = iZ_o/(V_{dc}/2)$, unit voltage $\bar{v} = v/(V_{dc}/2)$, unit time. $\bar{t} = t\omega_0$.

TABLE I
SPECIFICATIONS OF THE 7-kW HALF-BRIDGE NPC INVERTER PROTOTYPE

DC input voltage	$V_{dc}=800\text{V}$	Output voltage	$V_{o,rms}=164\text{V}$	Modulation index	$M=0.62$
Output power	$P_o=7\text{kW}$	Load current	$I_{o,rms}=42.5\text{A}$	Switching frequency	$f_c=6.5\text{kHz}$

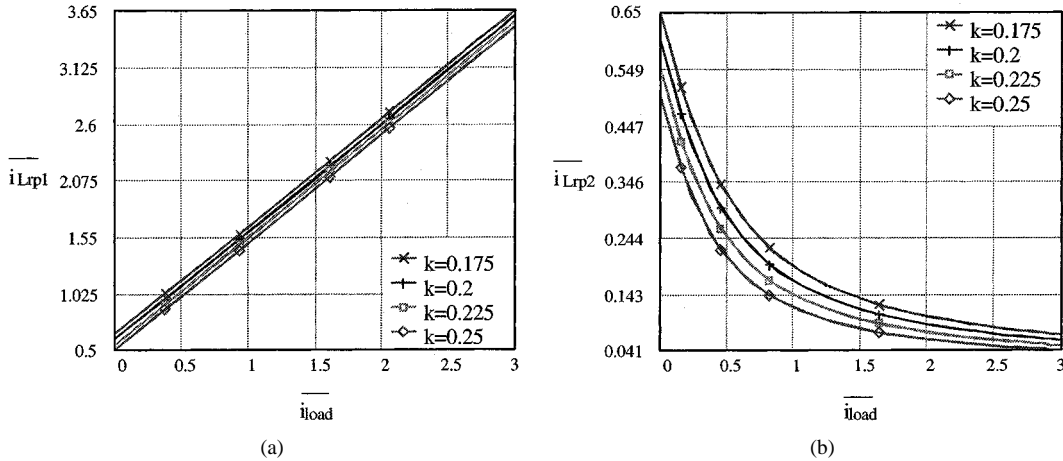


Fig. 7. Variations of the resonant inductor peak currents with load current and transformer ratio; mathematical expressions for i_{Lrp1} and i_{Lrp2} are given in Table II. (a) Diode-to-switch commutation. (b) Switch-to-diode commutation.

TABLE II
TOTAL COMMUTATION DURATION EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

	expressions	expressions in unit value
diode to switch commutation	$t_{s1} = L_r \frac{i_{load}}{(1-2k)(V_{dc}/2)} + \frac{\pi - \arccos\left(\frac{2kV_{dc}}{(1-2k)(V_{dc}/2)}\right)}{\omega_o} + \frac{L_r i_{load}}{Z_o 2kV_{dc}} + L_r \frac{i_{load}}{2kV_{dc}}$ <p style="text-align: center;">(1)</p>	$\omega_o t_{s1} = \frac{i_{load}}{(1-2k)} + (\pi - \arccos \frac{2k}{1-2k}) + \frac{\sqrt{1-4k}}{2k} + \frac{i_{load}}{2k}$ <p style="text-align: center;">(3)</p>
switch to diode commutation	$t_{s2} = \frac{\pi - \arccos \frac{2kV_{dc}}{\sqrt{(1-2k)^2 (V_{dc}/2)^2 + [i_{load} Z_o]^2}}}{\omega_o} + \frac{\arccos \frac{(1-2k)V_{dc}}{\sqrt{(1-2k)^2 (V_{dc}/2)^2 + [i_{load} Z_o]^2}}}{\omega_o} + L_r \frac{\sqrt{(1-2k)^2 (V_{dc}/2)^2 + [i_{load} Z_o]^2} - (2k)^2 (V_{dc}/2)^2 - i_{load} Z_o}{2k Z_o (V_{dc}/2)}$ <p style="text-align: center;">(2)</p>	$\omega_o t_{s2} = \pi - \arccos \frac{2k}{\sqrt{(1-2k)^2 + i_{load}^2}} - \arccos \frac{(1-2k)}{\sqrt{(1-2k)^2 + i_{load}^2}} + \sqrt{1-4k + i_{load}^2} - i_{load}$ <p style="text-align: center;">(4)</p>

- Circuit parasitics, device switching delays, losses, etc., are neglected in the analysis.

From Fig. 6, for diode-to-switch commutation, the commutation duration increases with load current but decreases with transformer ratio. For switch-to-diode commutation, it decreases with both load current and transformer ratio. From Fig. 7, for diode-to-switch commutation, the peak resonant

inductor current increases with load current but decreases with transformer ratio. For switch-to-diode commutation, it decreases with both load current and transformer ratio. Moreover, from Fig. 8, the resonant inductor rms current contributed from diode-to-switch commutation increases with load current, but decreases with transformer ratio and switching cycle. The resonant inductor rms current contributed from switch-to-diode

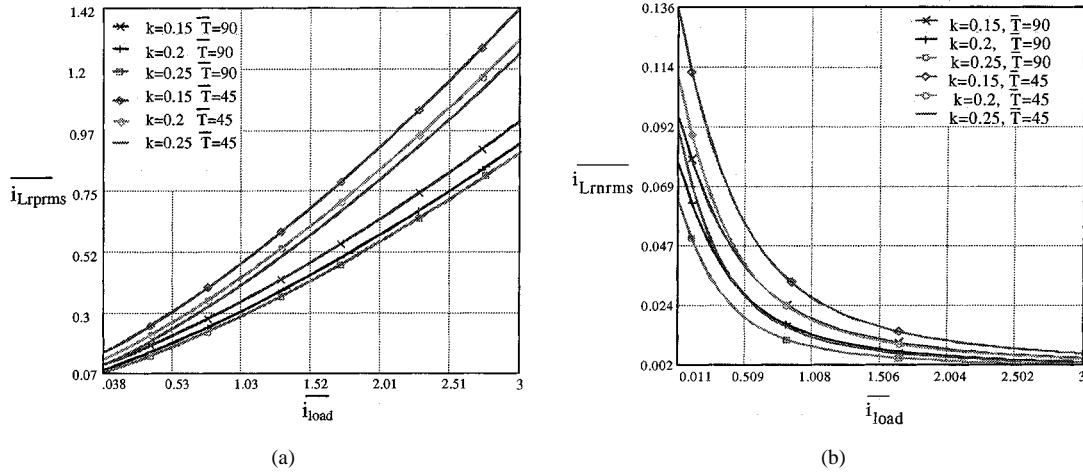


Fig. 8. Variations of the resonant inductor rms currents with load current, transformer ratio, and switching cycle; mathematical expressions for i_{Lrprms} and i_{Lrnrms} are given in Table III. (a) Diode-to-switch commutation. (b) Switch-to-diode commutation.

TABLE III
PEAK RESONANT CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

	actual expressions	expressions in unit value
diode to switch commutation	$i_{Lrp1} = i_{load} + \frac{\sqrt{(1-2k)^2 (V_{dc}/2)^2}}{Z_o} \quad (5)$	$\overline{i_{Lrp1}} = (\overline{i_{load}} + 1 - 2k) \quad (7)$
switch to diode commutation	$i_{Lrp2} = \frac{\sqrt{(1-2k)^2 (V_{dc}/2)^2 + [i_{load} Z_o]^2}}{Z_o} - i_{load} \quad (6)$	$\overline{i_{Lrp2}} = \sqrt{(1-2k)^2 + \overline{i_{load}}^2} - \overline{i_{load}} \quad (8)$

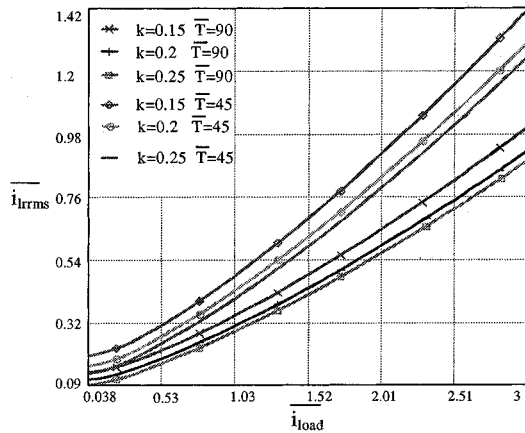


Fig. 9. Variations of the resonant inductor rms current with load current, transformer ratio, and switching cycle, $\overline{i_{irms}}^2 = \overline{i_{Lrprms}}^2 + \overline{i_{Lrnrms}}^2$; mathematical expressions for $\overline{i_{Lrprms}}$ and $\overline{i_{Lrnrms}}$ are given in Table IV.

commutation, however, decreases with load current, transformer ratio, and switching cycle. The synthesized resonant inductor rms current contributed from both diode-to-switch commutation and switch-to-diode commutation is given in Fig. 9, which increases with load current, but decreases with transformer ratio and switching cycle. Finally, the synthesized resonant capacitor rms current contributed from both diode-to-switch commutation and switch-to-diode commutation is shown in Fig. 10, it decreases with transformer ratio and switching cycle. For load current within 1-unit amplitude,

it decreases also with load current, beyond which, it becomes independent of the load current.

The reverse proportional relation of the commutation duration, resonant inductor peak current, and resonant inductor rms current with load current for switch-to-diode commutation highly justifies the auxiliary switch gating strategy in this paper to trigger the corresponding auxiliary switch simultaneously with the main switch not only for diode-to-switch commutation where such triggering is indispensable for achieving zero-voltage switching, but also for switch-to-diode commutation where such triggering becomes dispensable above certain load current level. Such triggering strategy facilitates significant control simplification while the extra loss so accrued during switch-to-diode commutation is negligible.

Note that the auxiliary switch rms current equals the diode to switch commutation component for one load current direction, and it equals the switch-to-diode commutation component for the other load current direction. As far the auxiliary diode in the transformer primary is concerned, the rms current stresses can be given accordingly from the transformer ratio.

For design of the auxiliary circuit, the transformer ratio should be set less than 1/4 dependent on the actual resonant loop resistance to ensure the pole voltage swinging to the rail level during the commutation resonance [18]. The resonant capacitance can be designed as per the device turn-off loss and the associated thermal condition [20]. Resonant inductance can then be decided according to the accepted resonant circuit rms current stress based on Fig. 9, taking into account the system

TABLE IV
RESONANT INDUCTOR RMS CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

	actual expressions	expressions in unit value
diode to switch commutation	$i_{Lrprms} = \sqrt{\frac{1}{T} \int_0^{k_p} i_{1p}^2 dt + \frac{1}{T} \int_0^{k_p} i_{2p}^2 dt + \frac{1}{T} \int_0^{k_p} i_{3p}^2 dt} \quad (9)$ <p>where:</p> $i_{1p} = \frac{(V_{dc}/2)(1-2k)}{L_r} t$ $k_{1p} = i_{load} \frac{L_r}{(1-2k)(V_{dc}/2)}$ $i_{2p} = i_{load} + (1-2k) \frac{(V_{dc}/2)}{Z_o} \sin(\omega_s t)$ $k_{2p} = \frac{\pi - a \cos(\frac{2k}{1-2k})}{\omega_s}$ $i_{3p} = \frac{(V_{dc}/2)}{Z_o} \sqrt{(1-2k)^2 - (2k)^2} + i_{load} - \frac{2kt}{L_r} (V_{dc}/2)$ $k_{3p} = \frac{L_r i_{load}}{2k(V_{dc}/2)} + \frac{L_r \sqrt{(1-2k)^2 - (2k)^2}}{2kZ_o}$	$(\bar{i}_{Lrprms})^2 = \frac{1}{T} \int_0^{\bar{k}_{1p}} [\bar{i}_{1p}(1-2k)\bar{t}]^2 d\bar{t}$ $+ \frac{1}{T} \int_0^{\bar{k}_{2p}} [\bar{i}_{load} + (1-2k)\sin(\bar{t})]^2 d\bar{t} + \frac{1}{T} \int_0^{\bar{k}_{3p}} [\sqrt{1-4k} + \bar{i}_{load} - 2k\bar{t}]^2 d\bar{t} \quad (10)$ <p>where:</p> $\bar{k}_{1p} = \bar{i}_{load} / (1-2k)$ $\bar{k}_{2p} = \pi - a \cos(\frac{2k}{1-2k})$ $\bar{k}_{3p} = (\bar{i}_{load} + \sqrt{1-4k}) / (2k)$
switch to diode commutation	$i_{Lrnrms} = \sqrt{\frac{1}{T} \int_0^{k_p} i_{1n}^2 dt + \frac{1}{T} \int_0^{k_p} i_{2n}^2 dt} \quad (11)$ <p>where:</p> $i_{1n} = i_{load} - \frac{(1-2k)\sin(\omega_s t)}{Z_o} (V_{dc}/2) - i_{load} \cos(\omega_s t)$ $k_{1n} = \frac{\pi - a \cos(\frac{2k}{1-2k})}{\omega_s}$ $i_{2n} = \frac{\sqrt{(V_{dc}/2)^2 [(1-2k)^2 - (2k)^2] + i_{load}^2 Z_o^2}}{Z_o} + i_{load} + \frac{2kt(V_{dc}/2)}{L_r}$ $k_{2n} = \frac{\sqrt{[(1-2k)^2 - (2k)^2](V_{dc}/2)^2 + i_{load}^2 Z_o^2} - i_{load} Z_o}{2kZ_o(V_{dc}/2)}$	$(\bar{i}_{Lrnrms})^2 = \frac{1}{T} \int_0^{\bar{k}_{1n}} [\bar{i}_{load} + (2k-1)\sin(\bar{t}) - \bar{i}_{load} \cos(\bar{t})]^2 d\bar{t}$ $+ \frac{1}{T} \int_0^{\bar{k}_{2n}} [\sqrt{1-4k} + (\bar{i}_{load})^2 + \bar{i}_{load} + 2k\bar{t}]^2 d\bar{t} \quad (12)$ <p>where:</p> $\bar{k}_{1n} = \pi - a \cos(\frac{2k}{1-2k}) - a \cos(\frac{1-2k}{\sqrt{(1-2k)^2 + (\bar{i}_{load})^2}})$ $\bar{k}_{2n} = (\sqrt{(1-2k)^2 + (\bar{i}_{load})^2} - \bar{i}_{load}) / (2k)$

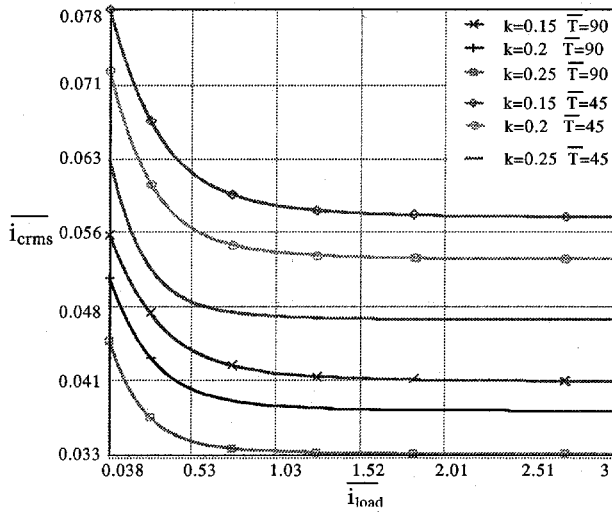


Fig. 10. Variations of the resonant capacitor rms current with load current, transformer ratio, and switching cycle, $\bar{i}_{crms}^2 = \bar{i}_{cprms}^2 + \bar{i}_{cnrms}^2$; mathematical expressions for \bar{i}_{cprms} and \bar{i}_{cnrms} are given in Table V.

operating frequency. Rating of the auxiliary switch or the auxiliary diode can be determined according to the rms current stress given in Fig. 8, and the peak current stress given in Fig. 7.

Gating signal width for the auxiliary switch must cover the maximum commutation duration given in Fig. 6 and remains constant over the low-frequency cycle. In the meantime, the minimum pulsewidth in the inverter PWM pattern should not

fall less than this duration. The next commutation should not start before the conclusion of the previous commutation.

On the other hand, transformer design can be based on the knowledge of commutation (magnetization) duration and the resonant inductor rms current stress. Particular attention is required keeping the magnetization current minimized. Meanwhile, with peak and rms resonant inductor current information, the resonant inductor can be designed.

IV. EXPERIMENTATION RESULTS

A 7-kW insulated gate bipolar transistor (IGBT) half-bridge NPC inverter prototype has been built. The specifications of which are given in Table I. Circuit parameters of the prototype are: $L_r = 12 \mu\text{H}$, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 0.1 \mu\text{F}$, $k = 0.2$. Auxiliary switch gating signal width is set at $14.4 \mu\text{s}$. Maximum and Minimum PWM widths are set at 136.8 and $16.8 \mu\text{s}$, respectively.

Main switches $S_1 - S_4$ and auxiliary switches $S_{a1} - S_{a4}$ used are Semikron SKM50GB123D (1200 V/50 A). Auxiliary diodes $D_{c1} - D_{c2}$ and $D_{ac1} - D_{ac2}$, used are ultrafast HFA30T60C (600 V/30 A). Inverter output is installed with a second-order filter $L_f = 1.45 \text{ mH}$ and $C_f = 12 \mu\text{F}$.

Four 350-V/3300- μF capacitors are used at the dc link. It is worth mentioning that the half-bridge prototype is modulated with normal subharmonic PWM pattern under which the neutral potential has been proved to be self-balancing when the load is not purely capacitive, due to the inherent feedback loop for the

TABLE V
 RESONANT CAPACITOR RMS CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

	actual expressions	expressions in unit value
diode to switch commutation	$i_{crms} = \sqrt{\frac{1}{T} \int_0^{kT} \left(\frac{(1-k)V_{dc} \sin(\omega_0 t)}{2Z_0} \right)^2 dt} \quad (13)$	$\bar{i}_{crms} = \sqrt{\frac{1}{T} \int_0^{kT} \left(\frac{(1-k)V_{dc} \sin(\bar{t})}{2} \right)^2 d\bar{t}} \quad (15)$
switch to diode commutation	$i_{cnms} = \sqrt{\frac{1}{T} \int_0^{kT} \left(\frac{i_{load}(1-\cos(\omega_0 t))}{2} + \frac{V_{dc}(k-1)\sin(\omega_0 t)}{2Z_0} \right)^2 dt} \quad (14)$	$\bar{i}_{cnms} = \sqrt{\frac{1}{T} \int_0^{kT} \left(\frac{i_{load}(1-\cos(\bar{t}))}{2} + \frac{(k-1)\sin(\bar{t})}{2} \right)^2 d\bar{t}} \quad (16)$

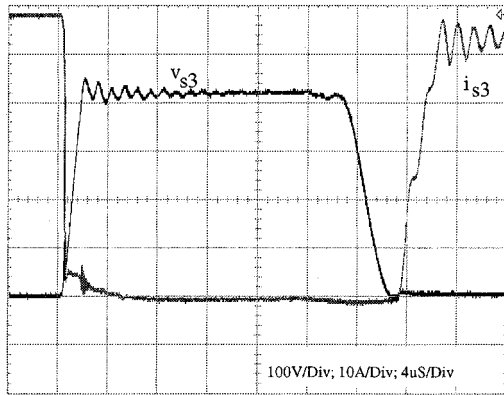


Fig. 11. Experimental waveforms of the main switch S_3 voltage and current during S_3-D_1 commutation and D_1-S_3 commutation.

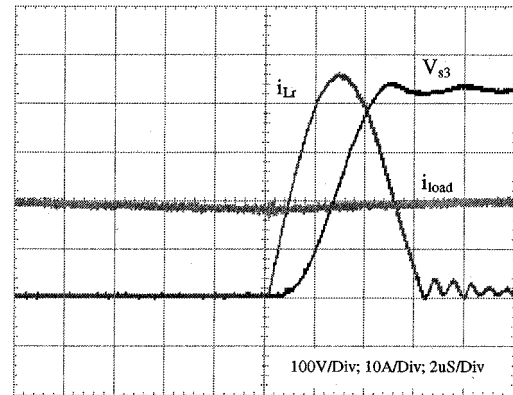


Fig. 13. Experimental waveforms of the main switch S_3 voltage, load current, and resonant inductor current during $D_{c1}-S_1$ commutation.

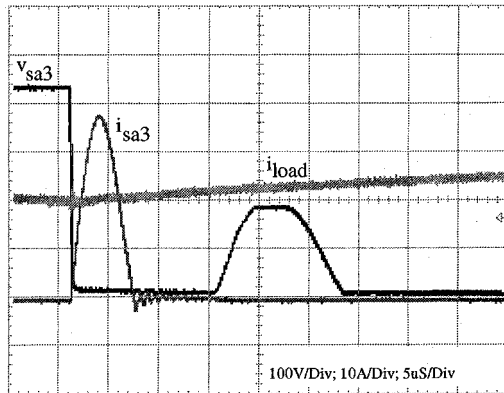


Fig. 12. Experimental waveforms of the auxiliary switch S_{a3} voltage and current as well as the load current during $D_{c1}-S_1$ commutation.

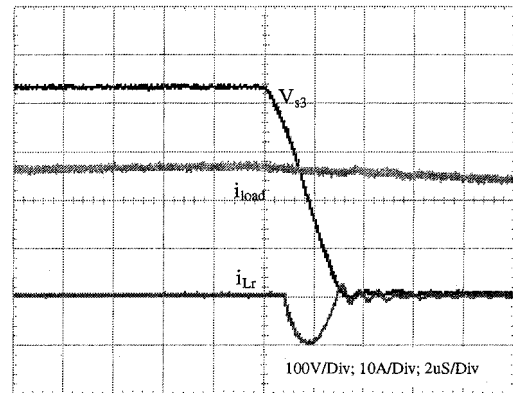


Fig. 14. Experimental waveforms of the main switch S_3 voltage, load current, and resonant inductor current during S_1-D_{c1} commutation.

dc current component flowing into the neutral potential [21]. No specific measures are taken for stabilizing the neutral potential.

Four simple zero-voltage detecting circuits [18] are employed to interface the four Semikron SKH10 drivers to the main IGBT switches for releasing the gating signals once the detected voltage reaches zero.

Fig. 11 shows the main device S_3 voltage and current waveforms during S_3-D_1 and D_1-S_3 commutation. Obviously, the

main device works with zero-voltage turn-on and capacitive turn-off. No voltage/current spikes are produced in the process. In the meanwhile, Fig. 12 shows the waveforms of the auxiliary switch S_{a3} voltage and current as well as the load current during D_{c1} to S_1 commutation. The auxiliary switch works with zero current turn-off and inductive turn-on, and no voltage spike is observed. With a predicted commutation duration of $7.2 \mu s$ according to Fig. 6(a) and a predicted peak resonant

current of 47.8 A according to Fig. 7(a) at load current of 20 A, the experimental values are 6.7 μ s and 40.5 A respectively. The analysis results presented in Section III are well validated. Further, detailed relationships among resonant inductor current, load current and main switch voltage during diode-to-switching commutation and switching-to-diode commutation are illustrated in Figs. 13 and 14. Minor errors occur due to the ohmic losses in the commutation processes neglected in the analysis. Measured prototype efficiency is 95%.

V. CONCLUSIONS

The analysis and experimentation presented verify that the proposed small-rating zero-current—switching auxiliary circuit guarantees the zero-voltage switching of the NPC main switches, without requiring any extra monitoring or controlling and without incurring any voltage/current spikes or modulation constraints. The auxiliary switches block the same voltage as the main switches. The scheme can be used to advantage for high-power high-frequency application of the NPC inverter where conventional snubber or hard switching is not expected to offer adequate performance.

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