Three-Phase Multilevel PWM Rectifiers Based on Conventional Bi-directional Converters

Marcelo L. Heldwein, *Member, IEEE*, Samir A. Mussa, *Member, IEEE*, and Ivo Barbi, *Senior member, IEEE*

Abstract—**Almost two decades of research on unidirectional three-phase three-level boost-type PWM rectifiers have shown the benefits of employing this technology to comply with power quality standards while assuring high efficiency and low volume and weight. However, the unidirectional topologies directly derived from the conventional three-level bi-directional converters, such as the Neutral Point Clamped (NPC), the Flying Capacitor and the Cascaded Full-bridge converters have not been properly analyzed. This work introduces some of the unidirectional topologies which arise from the inspection of the wide-spread conventional bi-directional converters. Special emphasis is put in the analysis of the Neutral Point Clamped based three-phase/-level PWM rectifier operating as power factor corrector.**

I. INTRODUCTION

UNIDIRECTIONAL three-phase/-level boost-type PWM rectifiers present, as shown in [1]–[4], offer considerable advantages over two-level rectifiers. They have found application where high quality input currents, high efficiency, low volume and weight are required and unidirectional converters are to be employed. This is due to the results achieved for the last two decades in, both, industrial and research institutions, where efficiencies close to 98% [3], [5] and very high power density [6], [7] have been reported. Power modules are commercially available [5], [8] providing the basis for industrial applications, such as in [9], [10]. Furthermore, extensive work has been carried out regarding modulation and control [11]–[14].

The unidirectional three-phase/-level boost-type PWM rectifiers are able to generate voltages with instantaneous average values which approach pure sinusoidal voltages at one end of the input inductors, from where the input currents flow in phase with the power grid phase voltages. Therefore, high quality current waveforms can be generated. The three-level operation allows the voltage steps to be lower than those found in two-level topologies, from where lower harmonic contents are observed. Thus, smaller input filters are allowed. In addition, the voltage across the semiconductors is, in theory, limited to half of what is typical in two-level topologies. This feature enables the use of semiconductors with lower voltage ratings, thus, with lower voltage drops for the same current ratings and reduces the switched voltages. With this, both, conduction and switching losses can be reduced. The overall result is that smaller/lighter cooling systems and passive components are employed when compared to two-level systems. However, modulation, control and voltage balancing challenges arise with the three-level topologies and make their design more complex, increasing the efforts in control hardware.

Researchers have generated different topologies that implement three-level operation and several of them have been reported in the literature [15]–[20]. Each of these, present some different characteristics, even though the obtainable input and output waveforms are basically the same. Nevertheless, the unidirectional topologies which derive directly from the traditional bi-directional three-level inverters, such as the Neutral Point Clamped (NPC), the Flying Capacitor and the Symmetric Cascaded H-Bridge have not yet been analyzed in the literature. This work introduces some of these topologies, while providing a basic analysis of their operation as three-phase PFC converters, pointing out the main benefits and drawbacks.

II. UNIDIRECTIONAL MULTILEVEL TOPOLOGIES

This section shows the derivation of unidirectional multilevel PWM rectifiers based on the widespread bi-directional multilevel converters known as the NPC, the Flying Capacitor and the Symmetric Cascaded H-Bridge.

A. Unidirectional Flying Capacitor Based PWM Rectifier

The Flying Capacitor (FC) inverter proposed in [21] is a well known multilevel PWM topology. One leg of a three-level FC converter is shown in Fig. 1(a), which allows for bi-directional power flow. Fig. 1(b) takes into consideration an unidirectional power flow from a current source connected at a to the output voltage source between p and n and shows that switches $S_{p,A}$ and $S_{A,n}$ are not required for this operation mode. Another equivalent topological variation would be to exclude $S_{A,p}$ and $S_{n,A}$. As shown in Table I, the circuit in Fig. 1(c) suffices for unidirectional operation.

The resulting topology presents the same characteristics as its preceding bi-directional one, except from the fact that the current through the flying capacitor i_{FC} is only positive for $i_a > 0$ and negative for $i_a < 0$. Therefore, the balancing strategy of such capacitor should consider this fact. A drawback of the three-phase topology is the requirement to balance more than two dc voltages. Conduction losses are expected to be low, since a low number of semiconductors is in series with the paths for the switched currents.

B. Symmetric Cascaded H-Bridge Based PWM Rectifier

Another widespread multilevel topology is the Symmetric Cascaded H-Bridge inverter [22], [23]. It is also possible to generate a unidirectional version based on a leg of the original

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The authors are with the Power Electronics Institute (INEP), Electrical Engineering Department, Federal University of Santa Catarina (UFSC), Florianópolis, SC, 88040-970, Brazil (e-mail: heldwein@inep.ufsc.br; samir@inep.ufsc.br; ivobarbi@inep.ufsc.br).

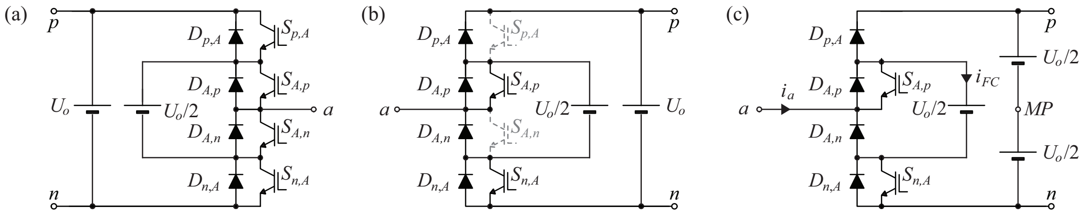

Fig. 1. Derivation of an unidirectional rectifier based on the (a) three-level Flying Capacitor inverter [21]. (b) Switches $S_{p,A}$ and $S_{A,n}$ are not required for rectifier only operation. (c) Leg of the FC based PWM rectifier topology.

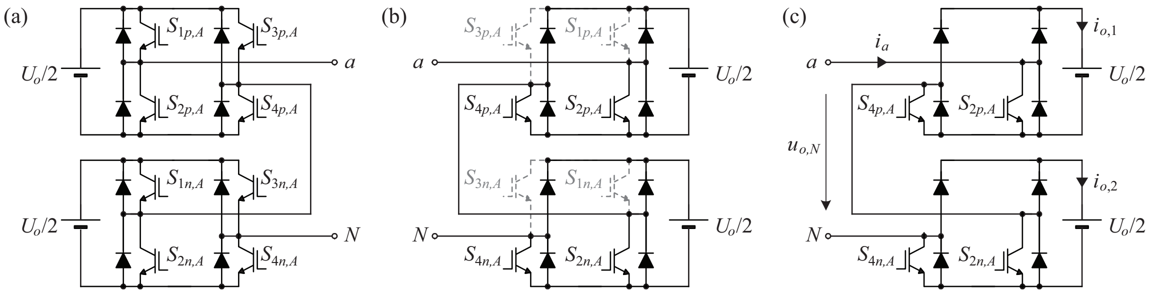

Fig. 2. Derivation of an unidirectional rectifier based on the (a) five-level Cascaded H-Bridge inverter [22], [23]. (b) Switches $S_{1p,A}$, $S_{3p,A}$ $S_{1n,A}$ and $S_{3n,A}$ are not required for rectifier only operation. (c) Leg of the cascaded H-bridge based PWM rectifier topology.

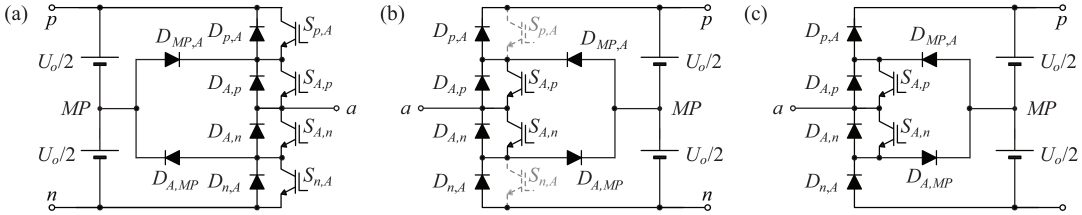

Fig. 3. Derivation of an unidirectional rectifier based on the (a) three-level NPC inverter [24]. (b) Switches $S_{p,A}$ and $S_{n,A}$ are not required for rectifier only operation. (c) Leg of the NPC based PWM rectifier topology.

topology as seen in Fig. 2 and in Table II, where two of the upper or lower switches can be excluded from each H-bridge cell. This leads to half of the number of turn-off switches when compared to the bi-directional version.

As the original topology, the unidirectional circuit requires isolated dc outputs that must be controlled. The main characteristics remain, so that the frequency at the input can be twice the switching frequency; any number of such cells can be stacked, so that this topology is highly modular; and, low conduction losses are expected.

C. Neutral Point Diode Clamped Based PWM Rectifier

The Neutral Point Clamped inverter proposed in [24], [25] is a bi-directional three-level PWM topology, which is widely employed in high power conversion. Fig. 3(a) shows one leg of such inverter. The DC-link is split into two equal voltages $U_o/2$ which limit the voltage across the switches $S_{p,A}$, $S_{A,p}$, $S_{A,n}$ and $S_{n,A}$ through the clamping diodes $D_{MP,A}$ and $D_{A,MP}$. Point a shall be connected to a current source, which is typically an interfacing inductor or an electrical machine. Inverting the drawing direction and considering the power flowing uniquely into the DC-link as shown in Fig. 3(b) causes no current to flow through switches $S_{p,A}$ and $S_{n,A}$, as shown in [26]. Therefore, for unidirectional rectifier operation the NPC topology can be reduced to the circuit shown in Fig. 3(c)

TABLE I

SWITCHING STATES FOR LEG A FOR THE FLYING CAPACITOR BASED TOPOLOGY (CF. FIG. 1(C)).

i_a	$S_{A,p}$	$S_{n,A}$	$u_{a,MP}$	i_{CF}
>0	—	0	$+U_o/2$	0
	—	1	0	$i_a(>0)$
<0	0	—	$-U_o/2$	0
	1	—	0	$i_a(<0)$

TABLE II

SWITCHING STATES FOR LEG A FOR THE SYMMETRIC CASCADED BASED TOPOLOGY (CF. FIG. 2(C)).

i_a	$S_{2p,A}$	$S_{4p,A}$	$S_{2n,A}$	$S_{4n,A}$	$u_{a,N}$	$i_{o,1}$	$i_{o,2}$
>0	0	—	0	—	$+U_o$	i_a	i_a
	0	—	1	—	$+U_o/2$	i_a	0
	1	—	0	—	$+U_o/2$	0	i_a
	1	—	1	—	0	0	0
<0	—	0	—	0	$-U_o$	$-i_a$	$-i_a$
	—	0	—	1	$-U_o/2$	$-i_a$	0
	—	1	—	0	$-U_o/2$	0	$-i_a$
	—	1	—	1	0	0	0

TABLE III
SWITCHING STATES FOR LEG A FOR THE NPC BASED TOPOLOGY (CF. FIG. 3(C)) IN DEPENDENCY OF THE INPUT CURRENT DIRECTION.

i_a	$S_{A,p}$	$S_{A,n}$	$u_{a,MP}$	i_{MP}
> 0	—	0	$+U_o/2$	0
	—	1	0	$i_a(> 0)$
< 0	0	—	$-U_o/2$	0
	1	—	0	$i_a(< 0)$

[26].

III. PFC OPERATION OF A THREE-PHASE/-LEVEL NPC BASED PWM RECTIFIER

The operation of the NPC based rectifier can be understood by examining Fig. 4 and Table III. It can be seen that diodes $D_{A,p}$ and $D_{p,A}$ conduct the input current when it is positive and switch $S_{A,n}$ is switched off. When the current is reversed and switch $S_{A,p}$ is on, the current flows through $S_{A,p}$ and $D_{MP,A}$. The other stages are complementary to these ones. It can also be seen that, if MOSFETs are employed, they can be switched on whenever the body diodes conduct in order to reduce the conduction losses in the diodes. For generating the input voltages at the input terminals, this topology presents the same voltage vectors as the topologies (cf. Table III) presented in [15], [18], [20] as well as the same characteristics regarding the balancing of the output voltages. Thus, all modulation and control schemes that have been proposed for these topologies can be directly employed here, including the balancing of the output voltages through the injection of a zero-sequence component in the current control signals.

A. Stresses in the Semiconductors

Considering the circuit in Fig. 5, the switched voltages across all semiconductors are clamped to the voltages $U_o/2$ across the DC-link capacitors $C_{o,p}$ and $C_{o,n}$.

Considering PFC operation and defining the input currents $i_J = I_{pk}\sin(\omega t + \phi_J)$ as ripple-free and the input voltages as $u_J = U_{pk}\sin(\omega t + \phi_J)$, where $J = A, B, C$ and $\phi_A = 0°$, $\phi_B = 120°$ and $\phi_C = 240°$. The modulation index M is defined as $M = \frac{2\,U_{pk}}{U_o}$. With these simplifications, the average and RMS currents are as defined in Table IV.

B. Comparison to a Standard Topology

The current efforts from the NPC-based topology can be directly compared to the ones of a standard topology [15]. Fig. 6) shows the topology under consideration and Table V gives the according current stresses. As the number of semiconductors is different, a comparison is performed by computing the total conduction losses from both topologies. The losses in the switches P_S and diodes P_D are given by

$$P_S = R_{ds,ON}\, I^2_{S,rms} \tag{1}$$

$$P_D = V_d\, I_{D,avg} + r_d\, I^2_{D,rms}, \tag{2}$$

where MOSFETs are chosen with $R_{ds,ON} = 0.11\,\Omega$, fast switching diodes with $V_{d,fast} = 0.90$ V and $r_{d,fast} = 120\,\mathrm{m}\Omega$ and slow switching diodes with $V_{d,slow} = 0.87$ V and $r_{d,slow} = 29\,\mathrm{m}\Omega$. A modulation index $M \cong 0.78$ is considered. The total conduction losses are computed as shown in Fig. 7, where the conduction losses for the NPC-based

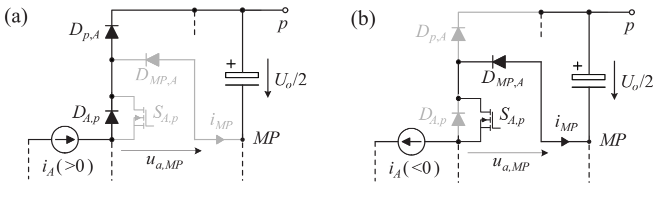

Fig. 4. Examples of operation stages for the NPC based PWM Rectifier.

TABLE IV
CURRENT STRESSES FOR THE NPC BASED RECTIFIER (CF. FIG. 3(C)).

Switches	*Average current*	*RMS current*
$S_{J,i}$, $D_{MP,J}$	$I_{pk}\left(\frac{1}{\pi} - \frac{M}{4}\right)$	$I_{pk}\sqrt{\frac{1}{4} - \frac{2M}{3\pi}}$
$D_{J,i}$, $D_{i,J}$	$I_{pk}\frac{M}{4}$	$I_{pk}\sqrt{\frac{2M}{3\pi}}$

TABLE V
CURRENT STRESSES FOR THE CONVENTIONAL RECTIFIER (CF. FIG. 6).

Switches	*Average current*	*RMS current*
$S_{J,i}$	$I_{pk}\left(\frac{1}{\pi} - \frac{M}{4}\right)$	$I_{pk}\sqrt{\frac{1}{4} - \frac{2M}{3\pi}}$
$D_{J,i}$	$I_{pk}\frac{1}{\pi}$	$I_{pk}\frac{1}{2}$
$D_{i,J}$	$I_{pk}\frac{M}{4}$	$I_{pk}\sqrt{\frac{2M}{3\pi}}$

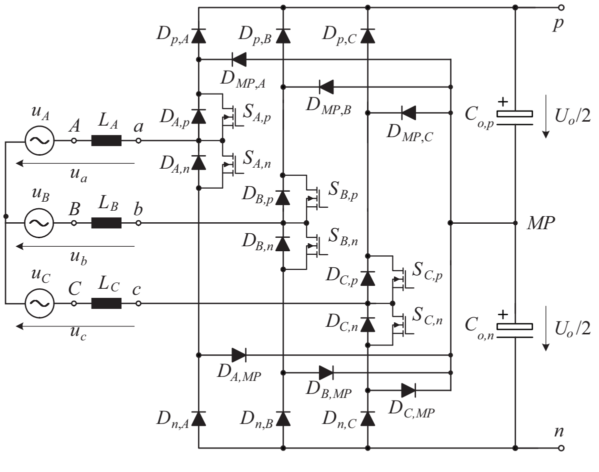

Fig. 5. The Three-Phase/-Level Neutral Point Clamped Based PWM Rectifier.

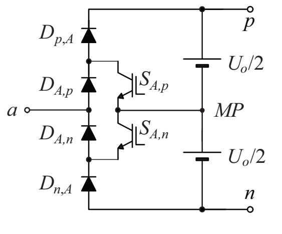

Fig. 6. Three-Phase/-Level rectifier proposed in [15].

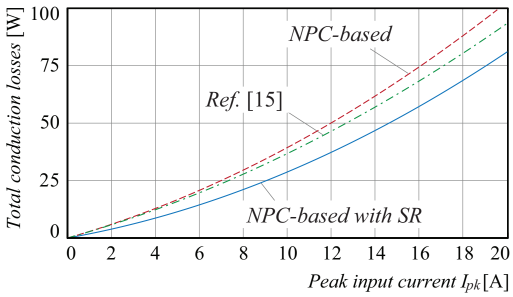

Fig. 7. Total conduction losses for the three-phase/-level rectifier proposed in [15] and for the NPC-based (cf. Fig. 3(c)) with and without synchronous rectification for $M = 0.78$.

converter are computed with and without applying gate-to-source voltages in the switches at the moments that diodes $D_{J,i}$ conduct. This is based on synchronous rectification (SR) schemes and significantly reduces conduction losses. The results obtained in Fig. 7 show that the conversion efficiency can be increased with the SR scheme applied to the NPC-based topology. On the other hand, not employing the SR scheme would lead to lower conduction losses for the standard topology proposed in [15]. Even though the body diode of the MOSFET is typically slower, switching losses are not expected to increase since fast diodes are in series with the MOSFETs body diode during switching intervals.

Considering IGBT based implementations for both converters, would cause the NPC-based topology to employ two extra diodes, whereas MOSFET based implementations would require the same number of semiconductors. Another difference among the topologies is that diodes $D_{J,i}$ are switched only once per mains cycle in the topology proposed in [15], where these diodes could be changed by thyristors and handle the pre-charge of the dc-link capacitors.

Regarding external characteristics, such as, control, variables to sense, dc-link voltages balancing, both topologies present the same behavior. However, depending on the switching speed of the semiconductors and on parasitic capacitances, the turn-off switches in the NPC-based topology are, in theory, subject to over-voltages during turn-off. In case this is observed, clamping circuits or avalanche rated devices are required.

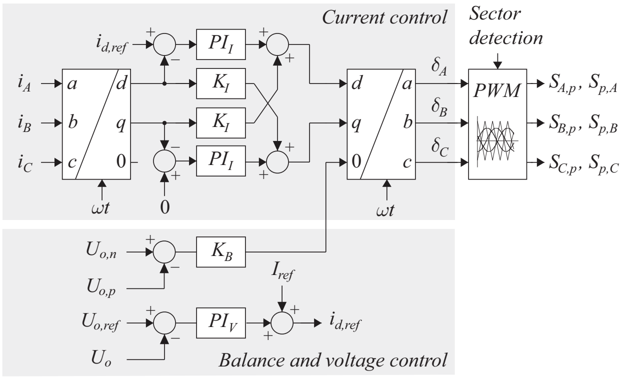

Fig. 8. Control simulation model for verifying PFC operation.

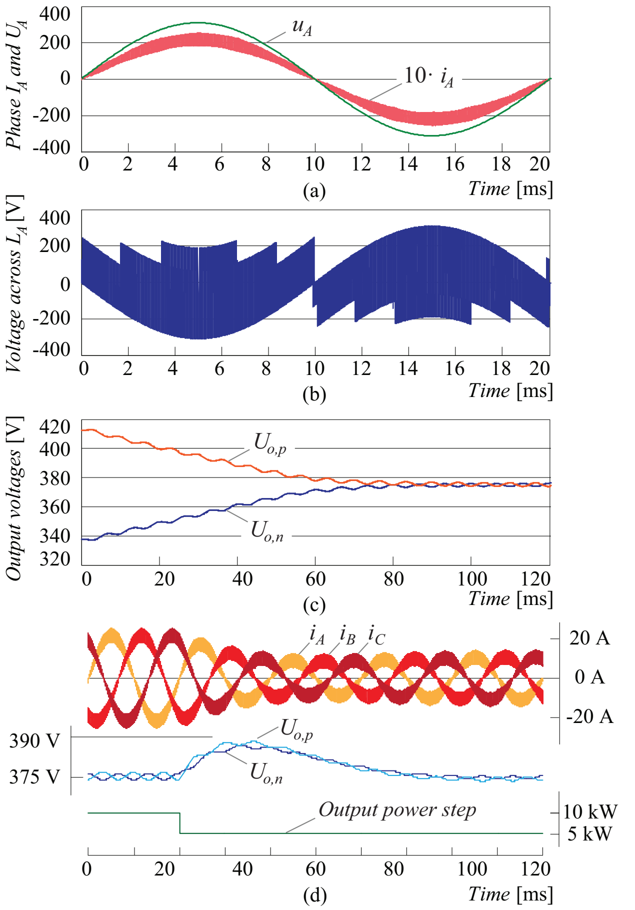

Fig. 9. Simulation results for verifying PFC operation: (a) Phase A input current i_A and voltage u_A; (b) voltage across the input inductor L_A; (c) output voltages $U_{o,p}$ and $U_{o,n}$ development after a 20% unbalance; and, (d) input currents, output voltages and power for a load step from 10 kW to 5 kW.

C. Closed Loop PFC Operation

In order to verify three-phase PFC operation, the circuits shown in Fig. 8 have been simulated. The following parameters have been employed: output reference voltage of $U_o = 750$ V, line-to-line mains voltages of 380 V, load step from rated power 10 kW to 5 kW at $t = 20$ ms, mains frequency $f_{mains} = 50$ Hz, switching frequency $f_s = 70$ kHz, input inductors $L_J = 160\ \mu$H, output capacitors $C_{o,p} = 2$ mF+10% and $C_{o,n} = 2$ mF$-$10%.

Fig. 9 shows simulations results for different operation conditions. Steady state waveforms for the phase voltage u_A and input current i_A are presented in Fig. 9(a) for 10 kW, from where it is seen that power factor correction is achieved. Fig. 9(b) depicts the voltage across the input inductor L_A for the same conditions. This voltage shows an advantage of the three-level operation, since the voltage steps are reduced when compared to a two-level converter. The voltage balance control loop acts to adjust the dc output voltages as observed in Fig. 9(c) for an initial unbalance of 20%. The output voltages and input currents are well controlled as shown in Fig. 9(d) for a load step from 10 kW to 5 kW.

IV. CONCLUSIONS

Forgotten topologies directly derived from three conventional bi-directional converters have been presented for unidirectional power flow. The Flying Capacitor and the Symmetric H-bridge topologies require a higher control effort, since they require more dc voltages to be stabilized. The unidirectional NPC based topology operating as PFC rectifier is analyzed in detail. It shows similar characteristics to more widespread three-level topologies and is an interesting alternative as a three-phase PFC rectifier. A synchronous rectification scheme has been proposed in order to lower conduction losses for the NPC-based rectifier.

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