

Novel Zero-Current-Switching PWM Converters

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Abstract— This paper presents a new family of pulsewidth-modulated (PWM) converters, featuring soft commutation of the semiconductors at zero current (ZC) in the transistors and zero voltage (ZV) in the rectifiers. Besides operating at constant frequency and with reduced commutation losses, these new converters have output characteristics similar to the hard-switching-PWM counterpart, which means that there is no circulating reactive energy that would cause large conduction losses. The new family of zero-current-switching (ZCS)-PWM converters is suitable for high-power applications using insulated gate bipolar transistors (IGBT's). The advantages of the new ZCS-PWM boost converter employing IGBT's, rated at 1.6 kW and operating at 20 kHz, are presented. This new ZCS operation can reduce the average total power dissipation in the semiconductors practically by half, when compared with the hard-switching method. This new ZCS-PWM boost converter is suitable for high-power applications using IGBT's in power-factor correction. The principle of operation, theoretical analysis, and experimental results of the new ZCS-PWM boost converter are provided in this paper to verify the performance of this new family of converters.

Index Terms— DC/DC converters, power electronics, soft-commutation techniques.

I. INTRODUCTION

SOFT-COMMUTATION techniques have been of great interest within the last few years in power-supply switching applications. However, frequency modulation, large conduction losses, and high voltage/current stresses in the switches are known drawbacks [1].

In order to overcome these difficulties, different authors have recently proposed alternative topologies. One of them, introduced in [2], uses an auxiliary switch to provide a dead time to temporarily interrupt the resonant transition. This technique has been generalized in [3]. Unfortunately, circulating reactive energy causes large conduction losses in these converters.

For high-power applications (above 1 kW) IGBT's are preferred, when compared with power MOSFET's, which present much higher conduction losses than IGBT's. On the other hand, IGBT's are relatively slow in switching speed, so the switching losses and the high frequency of operation are two well-known problems [4]. Therefore, to be able to operate at high frequency, ZVS or ZCS soft-commutation techniques are investigated for IGBT's in different topologies.

The zero-voltage-switching (ZVS) technique is presented in [5] and [6], and the performance of the zero-voltage-transition power-factor converter (ZVT-PFC) using IGBT's is analyzed in [6]. The auxiliary cell proposed in [5] incorporates the advantages of offering soft commutation for the main switch (ZVS) and auxiliary switch (ZCS). The current through the auxiliary switch becomes zero naturally, and the main switch is gated as a dual thyristor. The zero-voltage-transition pulsewidth-modulated (ZVT-PWM) boost converter proposed in [6] allows soft commutation (ZVS) for the main switch. However, in this circuit, the auxiliary switch does not benefit from the soft commutation (ZCS), and the control technique demands an independent gate circuit for the auxiliary switch. In addition, although the turn-on losses are eliminated using IGBT's at the main switch in [5] and [6], the turn-off losses are not zero, due to the presence of the current tail in IGBT's.

A comparative study of switching losses of IGBT's under soft switching (ZVS and ZCS) and hard switching is presented in [7]. The ZVS technique eliminates the turn-on losses, but, during the turn-off process, the presence of the current tail causes high turn-off losses, particularly for slow devices. So, this technique can be applied only to fast IGBT's with small current tails. Furthermore, those results verify that the turn-off losses in ZCS were significantly reduced, but the turn-on losses were practically the same as those for the hard-switching technique.

In this paper, a new principle is presented to achieve ZCS at constant frequency (ZCS-PWM) for the active switches and ZVS for the passive switches, with practically zero turn-on and turn-off losses, without an increase in their voltage and current stresses. This new ZCS technique is much more effective than ZVS techniques in reducing switching losses.

The new ZCS-PWM boost converter, using IGBT's rated at 1600 W and operating at 20 kHz, is used as an example to illustrate the operation of the new ZCS-PWM converters.

II. THE NEW ZCS-PWM CELL

Fig. 1(a) shows the new ZCS-PWM proposed cell. It is formed by two switches $S1$ and $S2$, two diodes $D1$ and $D2$, two resonant inductors L_{r1} and L_{r2} , and one resonant capacitor C_r . $S1$ is the main switch, which is responsible for the power transferred to the load, while $S2$ is an auxiliary switch that handles a small fraction of the total output power and is rated at a small average current.

Fig. 1(b) shows the new ZCS-PWM boost converter generated from the new ZCS-PWM cell. One can notice that the frequency-modulated quasi-resonant-ZCS boost converter

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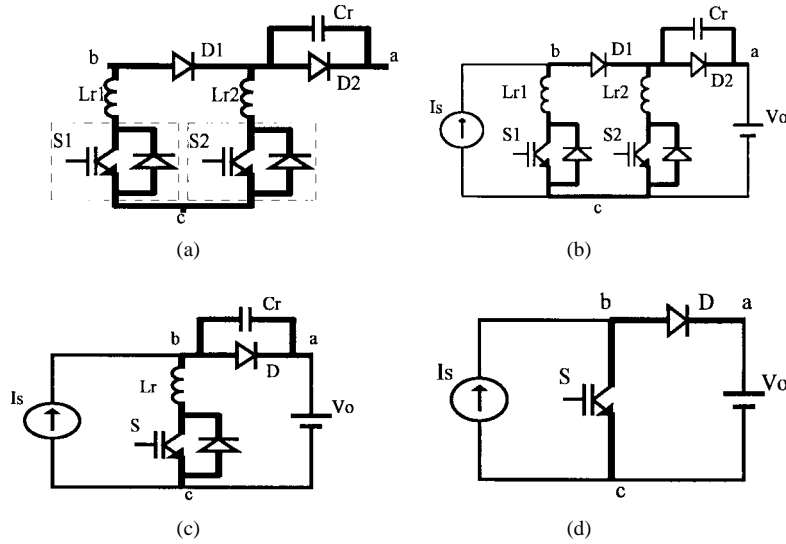


Fig. 1. (a) The new three-terminal ZCS-PWM cell. (b) New ZCS-PWM boost converter. (c) FM-ZCS-QRC. (d) Conventional hard-switching-PWM boost converter.

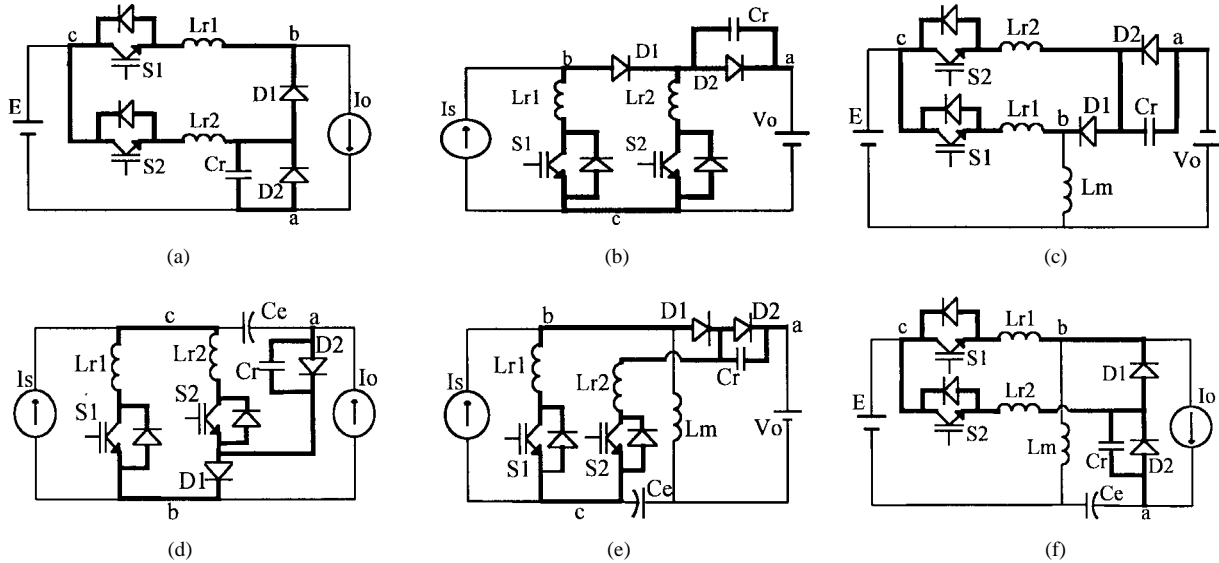


Fig. 2. The six basic topologies of the new ZCS-PWM converters. (a) Buck. (b) Boost. (c) Buck-boost. (d) Cuk. (e) Sepic. (f) Zeta.

(FM-ZCS-QRC) in Fig. 1(c) can be derived from the new ZCS-PWM converter, and the conventional hard-switching-PWM boost converter in Fig. 1(d) can be derived from the FM-ZCS-QRC. Therefore, the new ZCS-PWM converter is a more general topology, and it incorporates the most desirable properties of the previous circuits, namely, low conduction losses and PWM from the conventional converter and soft commutation from the ZCS-QRC.

III. THE NEW FAMILY OF ZCS-PWM CONVERTERS

The six basic new ZCS-PWM converters shown in Fig. 2 are generated from the proposed commutation cell shown in Fig. 1(a).

It should be noted that the principle of operation and features of these new converters are the same as those of the new ZCS-PWM boost converter.

In order to explain the operation and to simplify the analysis of these new ZCS-PWM converters, the new ZCS-PWM boost converter [Figs. 1(b) and 2(b)] is taken as an example. Therefore, it is assumed that the converter is operating in steady state, the input filter is large enough to be approximated by a current source I_s , the output voltage V_o is constant, and all components are ideal.

A. Stages of Operation of the New ZCS-PWM Boost Converter

Fig. 3 shows the nine topological stages of operation of the new ZCS-PWM boost converter, in agreement with the main waveforms shown in Fig. 4, where the main switch S_1 starts conducting at $t = t_0$ and the auxiliary switch S_2 at $t = t_2$. Both switches turn off simultaneously during the time interval $\Delta t_6 = t_6 - t_5$.

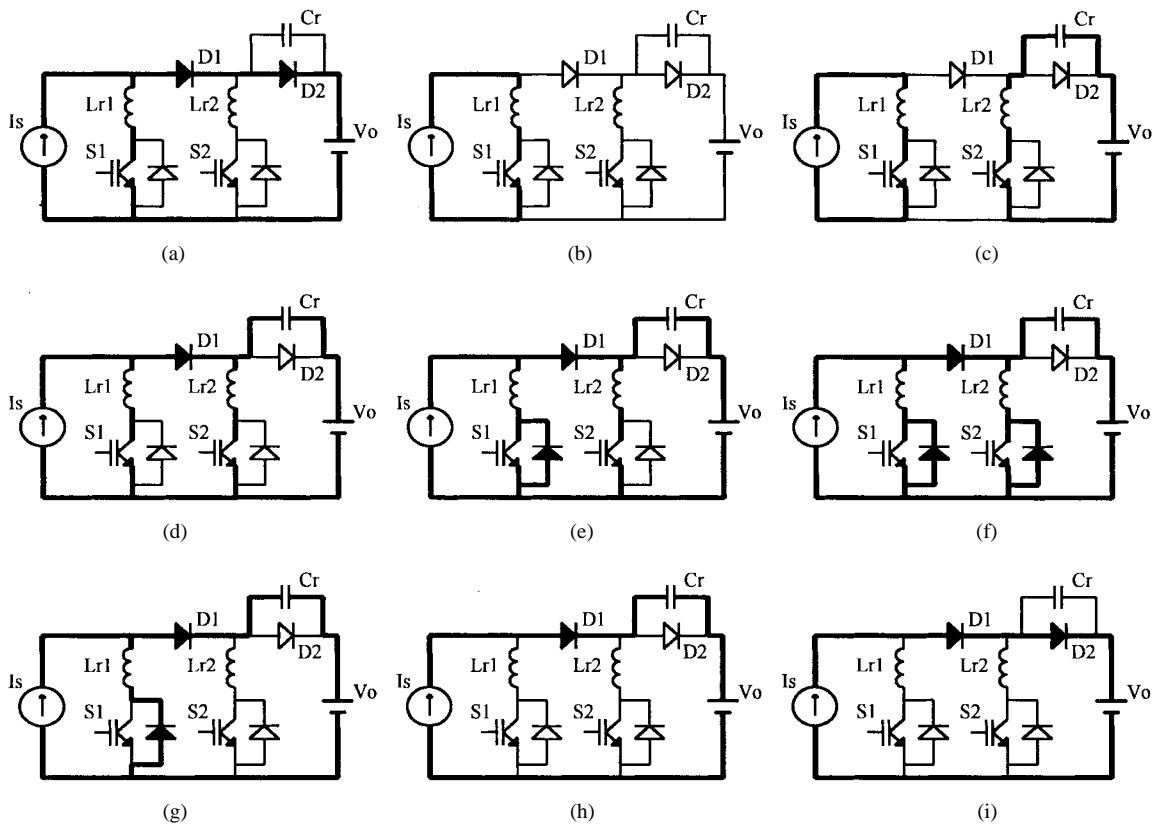


Fig. 3. The topological stages of the new ZCS-PWM boost converter.

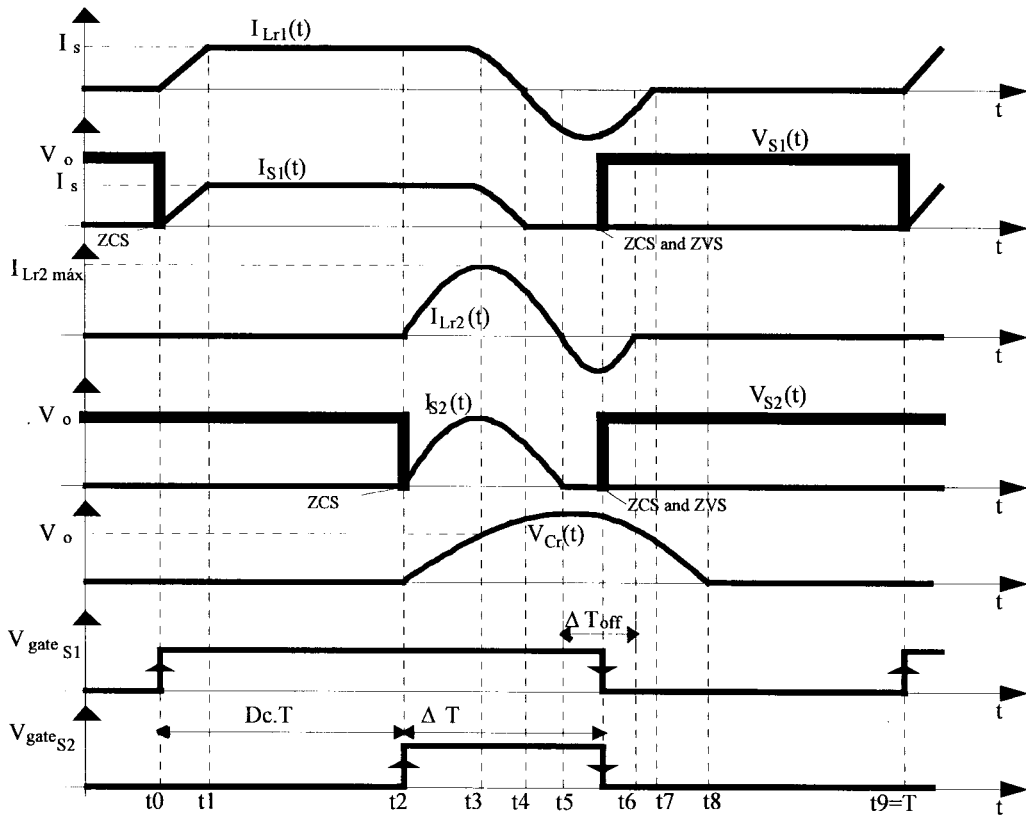


Fig. 4. Ideal relevant waveforms of the new ZCS-PWM boost converter.

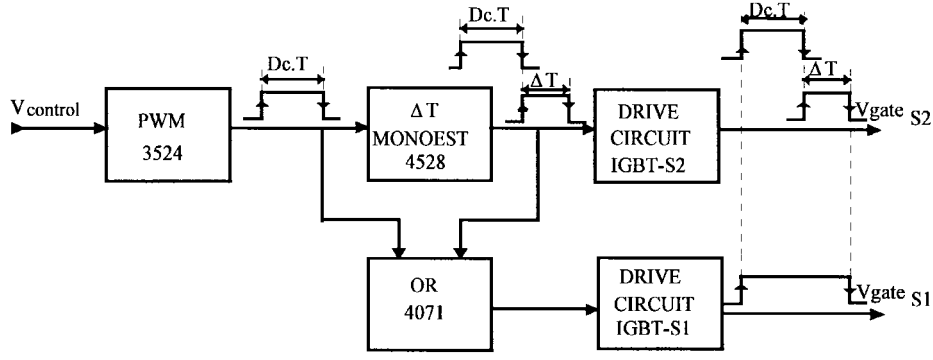


Fig. 5. Control timing diagram for the new ZCS-PWM boost converter.

Fig. 4 shows the ideal relevant waveforms for this new ZCS-PWM proposed boost converter during one switching cycle.

As can be seen in Fig. 4, the zero-current switching is achieved for the main ($S1$), and auxiliary ($S2$) switches. It should be noticed that the rectifier diodes ($D1$ and $D2$) were also softly commutated under zero-voltage switching.

From Fig. 4, it can be seen that the zero-current switching transition takes place only during the switching intervals, and the ZCS time interval ΔT is a small fraction of the switching period. The time interval ΔT depends on the resonant parameters and is independent of the output power.

Fig. 5 shows the control timing diagram proposed for the new ZCS-PWM boost converter. It is in agreement with the ideal waveforms shown in Fig. 4.

In order to perform the analysis and derive equations independent of particular parameter values, the parameters α and β are defined as follows:

$$\alpha = \frac{I_s}{V_o} \sqrt{\frac{L_{r2}}{C_r}} \quad (1)$$

$$\beta = \frac{L_{r2}}{L_{r1}}. \quad (2)$$

STAGE 1: $[t_0, t_1]$, Fig. 3(a).

Prior to the turn on of $S1$, the current I_s flows through $D1, D2$, and V_o . At the instant t_0 $S1$ is gated ON, to start stage 1. In this stage, i_{Lr1} rises linearly from zero up to I_s , while i_{D1} and i_{D2} fall toward zero. The time interval Δt_1 is given by (5):

$$i_{Lr1}(t) = \frac{V_o}{L_{r1}} t \quad (3)$$

$$i_{Lr2}(t) = V_{Cr}(t) = 0 \quad (4)$$

$$\Delta t_1 = \frac{1}{\omega_{01}} \frac{\alpha}{\beta} \quad (5)$$

where

$$\omega_{01} = \frac{1}{\sqrt{L_{r2} C_r}}. \quad (6)$$

Thanks to the presence of L_{r1} , during the commutation from $D1$ and $D2$ to $S1$, there are no switching losses.

STAGE 2: $[t_1, t_2]$, Fig. 3(b).

In this stage, the current I_s remains flowing through L_{r1} and $S1$. The remaining semiconductors are in the OFF state. The time interval Δt_2 is defined by (9):

$$i_{Lr1}(t) = I_s \quad (7)$$

$$i_{Lr2}(t) = V_{Cr}(t) = 0 \quad (8)$$

$$\Delta t_2 = DcT - \Delta t_1 \quad (9)$$

where Dc is the duty cycle of control, $T = 1/f_s$ is the switching period, and f_s is the switching frequency.

STAGE 3: $[t_2, t_3]$, Fig. 3(c).

At the instant t_2 , $S2$ is turned on. The current i_{Lr2} evolves in a resonant way, through V_o, C_r, L_{r2} , and $S2$. $S1$ remains conducting the current I_{S1} . Once again, due to the presence of L_{r2} , $S2$ is turned on with no switching losses. This stage ends when $V_{Cr}(t) = V_o$ at $t = t_3$. The time interval Δt_3 , and the current through L_{r2} at $t = t_3$ are given by (13) and (14), respectively:

$$i_{Lr1}(t) = I_s \quad (10)$$

$$i_{Lr2}(t) = \frac{I_s}{\alpha} \sin \omega_{01} t \quad (11)$$

$$V_{Cr}(t) = V_o(1 - \cos \omega_{01} t) \quad (12)$$

$$\Delta t_3 = \frac{1}{\omega_{01}} \frac{\pi}{2} \quad (13)$$

$$i_{Lr2}(t_3) = \frac{I_s}{\alpha}. \quad (14)$$

STAGE 4: $[t_3, t_4]$, Fig. 3(d).

At the instant t_3 , $D1$ also starts conducting. V_{Cr}, i_{Lr1} , and i_{Lr2} change in a resonant way. L_{r1} and L_{r2} are connected in parallel. Stage 4 ends when $i_{Lr1}(t) = 0$ at $t = t_4$:

$$i_{Lr1}(t) = I_s - \frac{\beta}{(1+\beta)} \frac{I_s}{\alpha} [1 - \cos \omega_{02} t] \quad (15)$$

$$i_{Lr2}(t) = \frac{I_s}{\alpha} - \frac{1}{(1+\beta)} \frac{I_s}{\alpha} [1 - \cos \omega_{02} t] \quad (16)$$

$$V_{Cr}(t) = V_o \left(1 + \frac{1}{\sqrt{1+\beta}} \sin \omega_{02} t \right) \quad (17)$$

where

$$\omega_{02} = \omega_{01} \sqrt{1+\beta}. \quad (18)$$

The voltage across C_r at $t = t_4$ and the time interval Δt_4 are given by (19) and (20), respectively:

$$V_{Cr}(t_4) = V_o \left(1 + \frac{1}{\beta} \sqrt{2\alpha\beta - \alpha^2 - \alpha^2\beta} \right) \quad (19)$$

$$\Delta t_4 = \frac{1}{\omega_{02}} a \cos \left[1 - \frac{\alpha(1+\beta)}{\beta} \right]. \quad (20)$$

STAGE 5: $[t_4, t_5]$, Fig. 3(e).

During this stage, the current I_{Lr1} changes its direction and flows through the antiparallel diode of $S1$. This stage ends when $I_{Lr2}(t) = 0$ at $t = t_5$. The time interval Δt_5 is governed by (21):

$$\Delta t_5 = \frac{1}{\omega_{02}} \left\{ a \cos(-\beta) - a \cos \left[1 - \frac{\alpha(1+\beta)}{\beta} \right] \right\}. \quad (21)$$

STAGE 6: $[t_5, t_6]$, Fig. 3(f).

During this stage, the current I_{Lr2} flows through the antiparallel diode of $S2$. This stage finishes at the instant $t = t_6$, when I_{Lr2} reaches zero. During this time interval, $S1$ and $S2$ are turned off at zero current and zero voltage. The current through L_{r1} at $t = t_6$ and the time interval Δt_6 are given by (22) and (23), respectively:

$$I_{Lr1}(t_6) = I_s \left(1 - \frac{\beta}{\alpha} \right) \quad (22)$$

$$\Delta t_6 = \frac{2}{\omega_{02}} [\pi - a \cos(-\beta)]. \quad (23)$$

STAGE 7: $[t_6, t_7]$, Fig. 3(g).

In stage 7, a resonant current flows through the antiparallel diode of $S1$. This stage ends when $I_{Lr1}(t) = 0$ at $t = t_7$. The time interval Δt_7 is given by (28):

$$I_{Lr1}(t) = \frac{I_s}{\alpha} [\alpha + \sqrt{\beta(1-\beta)} \sin \omega_{03}t - \beta \cos \omega_{03}t] \quad (24)$$

$$I_{Lr2}(t) = 0 \quad (25)$$

$$V_{Cr}(t) = V_o [1 - \sqrt{1-\beta} \cos \omega_{03}t - \sqrt{\beta} \sin \omega_{03}t] \quad (26)$$

where

$$\omega_{03} = \omega_{01} \sqrt{\beta} \quad (27)$$

$$\Delta t_7 = \frac{1}{\omega_{03}} \left\{ a \sin \left[\sqrt{\beta - \alpha^2} - \alpha \sqrt{\frac{1-\beta}{\beta}} \right] \right\}. \quad (28)$$

STAGE 8: $[t_7, t_8]$, Fig. 3(h).

In this stage, the input current I_s flows through $D1$ and C_r . Therefore, V_{Cr} decreases linearly toward zero, which is reached at the instant $t = t_8$. The time interval Δt_8 is given by (31):

$$I_{Lr1}(t) = I_{Lr2}(t) = 0 \quad (29)$$

$$V_{Cr}(t) = V_{Cr}(t_7) - \frac{I_s}{C_r} t \quad (30)$$

$$\Delta t_8 = \frac{1}{\omega_{01}} \frac{1}{\alpha} [1 - \sqrt{1-\beta} \cos \omega_{03} \Delta t_7 - \sqrt{\beta} \sin \omega_{03} \Delta t_7]. \quad (31)$$

STAGE 9: $[t_8, t_9]$, Fig. 3(i).

In this stage, the current I_s flows through $D1$, $D2$, and load. This stage ends at $t = t_9$, when $S1$ is gated ON to start the next operation period. The time interval Δt_9 is governed by (34):

$$I_{Lr1}(t) = I_{Lr2}(t) = 0 \quad (32)$$

$$V_{Cr}(t) = 0 \quad (33)$$

$$\Delta t_9 = T(1 - Dc) - \left[\sum_{i=3}^8 \Delta t_i \right]. \quad (34)$$

From Fig. 4, it can be seen that the zero-current switching is achieved for the active switches. In addition, it should be noticed that the control timing of the auxiliary switch and the soft-switching condition are independent of the output power. Therefore, the zero-current switching is achieved for the active switches, from nonload up to full load.

B. Output Characteristics

The dc voltage-conversion ratio (q) is defined by (35):

$$q = \frac{I_s}{I_o} = \frac{V_o}{V_{in}} \quad (35)$$

where V_{in} is the input voltage and I_o is the output current.

The output current (I_o) is governed by (36):

$$I_o = \frac{1}{T} \left\{ \int_0^{\Delta t_1} [I_s - I_{Lr1}(t)] dt - \int_0^{\Delta t_3} I_{Lr2}(t) dt - \int_0^{\Delta t^*} I_{Cr}(t) dt + \int_0^{\Delta t_7} [I_s - I_{Lr1}(t)] dt + \int_0^{\Delta t_8} I_s dt + \int_0^{\Delta t_9} I_s dt \right\} \quad (36)$$

where

$$\Delta t^* = \Delta t_4 + \Delta t_5 + \Delta t_6 \quad (37)$$

$$I_{Cr}(t) = C_r \frac{d}{dt} \left\{ V_o \left[1 + \frac{\sin(\omega_{02}t)}{\sqrt{1+B}} \right] \right\}. \quad (38)$$

Thus,

$$I_o = I_s(1 - Dc) - \frac{I_s}{2\pi f_{01}} \left\{ \frac{2\beta - \alpha^2}{2\alpha\beta} + A - B + \frac{\omega_{03} \Delta T_7}{\sqrt{\beta}} \right\} \frac{1}{f_s} \quad (39)$$

where

$$f_{01} = \frac{\omega_{01}}{2\pi} \quad (40)$$

$$A = \frac{\pi}{2} + \frac{[2\pi - a \cos(-\beta)]}{\sqrt{1+\beta}} \quad (41)$$

$$B = \frac{1}{\alpha} (\sqrt{\beta} \sin \omega_{03} \Delta t_7 + \sqrt{1-\beta} \cos \omega_{03} \Delta t_7). \quad (42)$$

With the above equations, the dc-voltage conversion ratio (q) is given by (43):

$$q = \frac{I_s}{I_o} = \frac{V_o}{V_{in}} = \frac{1}{1 - F(\alpha, \beta, f, Dc)} \quad (43)$$

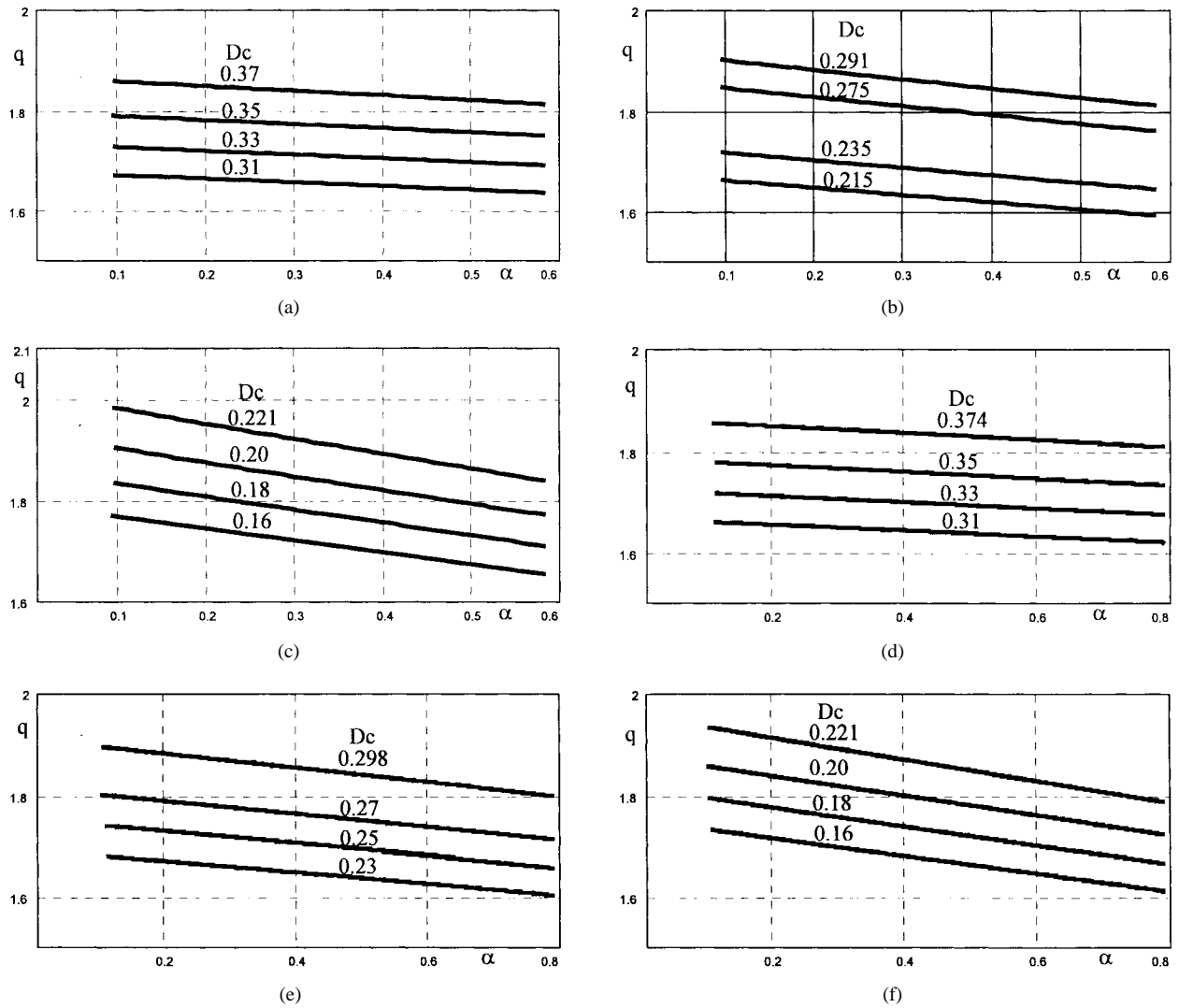


Fig. 6. Theoretical output characteristics for the new ZCS-PWM boost converter. (a) $\beta = 0.6$ and $f = 0.1$. (b) $\beta = 0.6$ and $f = 0.2$. (c) $\beta = 0.6$ and $f = 0.3$. (d) $\beta = 0.8$ and $f = 0.1$. (e) $\beta = 0.8$ and $f = 0.2$. (f) $\beta = 0.8$ and $f = 0.3$.

where

$$F(\alpha, \beta, f, Dc) = Dc + \frac{f}{2\pi} \left\{ \frac{2\beta - \alpha^2}{2\alpha\beta} + A - B + \frac{\omega_{03}\Delta t_7}{\sqrt{\beta}} \right\} \quad (44)$$

$$f = \frac{f_s}{f_{01}}. \quad (45)$$

It should be noticed that the analysis was developed in continuous-current mode (CCM). Therefore, the following constraint for the parameter α to maintain the CCM operation should be satisfied:

$$\alpha > \alpha_{\text{critic}} = \frac{(q-1)}{q^2 2L_f f_s} \sqrt{\frac{L_{r2}}{C_r}} \quad (46)$$

where L_f is the boost input inductance.

Fig. 6 shows the dc-voltage conversion ratio (q) for different values of the parameters β and f , as a function of the α parameter for this new ZCS-PWM boost converter. Furthermore, the dc-voltage conversion ratio for the novel ZCS-PWM converters are summarized in Table I.

TABLE I
DC-VOLTAGE CONVERSION RATIO OF THE NEW ZCS-PWM CONVERTERS

ZCS-PWM	Buck	Boost	Buck-boost, Cuk, Sepic, and Zeta
q	$F(\alpha, \beta, f, Dc)$	$\frac{1}{1-F(\alpha, \beta, f, Dc)}$	$\frac{F(\alpha, \beta, f, Dc)}{1-F(\alpha, \beta, f, Dc)}$

C. Commutation Analysis

In order to achieve soft commutation at zero-current switching for both active switches, for the described operation mode, the following inequalities should be satisfied:

$$\beta = \frac{L_{r2}}{L_{r1}} < 1 \quad (47)$$

and

$$\alpha < \beta. \quad (48)$$

The time interval Δt_{off} to turn off the switches $S1$ and $S2$ simultaneously is governed by (49). So, the time interval ΔT

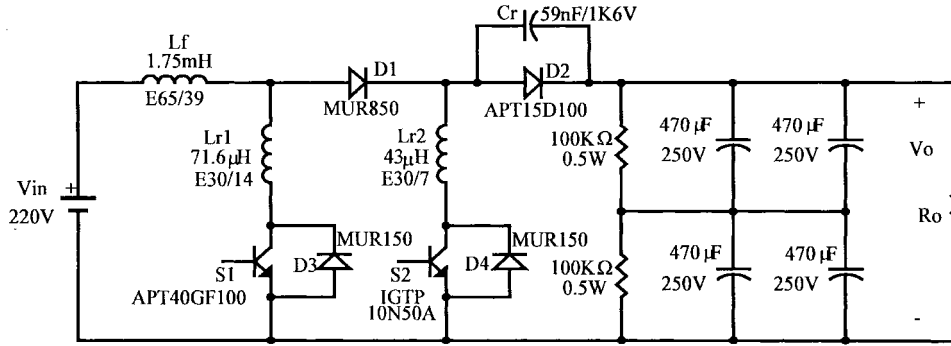


Fig. 7. Implemented circuit of the new ZCS-PWM boost converter.

for the control of the auxiliary switch is defined by (50):

$$\Delta t_{\text{off}} = \Delta t_G = \frac{1}{\omega_{01}} \left\{ \frac{2[\pi - a \cos(-\beta)]}{\sqrt{1+\beta}} \right\} \quad (49)$$

$$\Delta T = \frac{1}{\omega_{02}} \left[\frac{\pi\sqrt{1+\beta}}{2} + 2\pi - a \cos(-\beta) \right] - \frac{\Delta t_{\text{off}}}{2}. \quad (50)$$

Thus,

$$\Delta T = \frac{1}{\omega_{01}} \left[\frac{\pi}{2} + \frac{\pi}{\sqrt{1+\beta}} \right]. \quad (51)$$

Due to PWM operation, and to minimize the influence of the resonant parameters for the described operation mode, the following constraint should be satisfied through design procedure:

$$f = \frac{f_s}{f_{01}} < \frac{2\pi(1-Dc)}{\left\{ \frac{1}{\alpha} + A - B + \frac{\omega_{03}\Delta t_7}{\sqrt{\beta}} \right\}}. \quad (52)$$

IV. DESIGN PROCEDURE AND EXAMPLE

The design procedure and example of the new ZCS-PWM boost converter, taken as an example, is described as follows.

■ **Step 1**—Input and output data specifications.

$V_{\text{in}} = 220$ V (input voltage); $V_o = 400$ V (output voltage); $P_{\text{out}} = 1600$ W; $\eta = 0.95$ (minimum value of efficiency), and $f_s = 20$ kHz.

■ **Step 2**—Nominal input current ($I_{s_{\text{nom}}}$).

With the parameters shown in Step 1, the nominal input current is given by

$$I_{s_{\text{nom}}} = \frac{P_{\text{out}}}{\eta V_{\text{in}}} \cong 7.65 \text{ A}. \quad (53)$$

■ **Step 3**—Calculation of the resonant parameters.

In order to minimize the influence of the resonant parameters, and to satisfy the constraints for this operation mode, we selected the data from Fig. 6(b), where

$$\beta = 0.6; \quad \alpha_{\text{max}} = 0.55, \quad \text{and} \quad f = \frac{f_s}{f_{01}} = 0.2.$$

Therefore, with these parameters and (1), (2), (6), and (53), we can obtain the resonant parameters. Thus,

$$L_{r1} = 71.6 \mu\text{H}; \quad L_{r2} = 43 \mu\text{H}, \quad \text{and} \quad C_r = 59 \text{ nF}.$$

Furthermore, with the parameters listed above, from (1) one can obtain $\alpha_{\text{max}} \cong 0.51$.

■ **Step 4**—Maximum value of the current through L_{r2} ($I_{Lr2_{\text{max}}}$).

With (14) and the parameters from the above steps, we can obtain the $I_{Lr2_{\text{max}}}$ value. Thus,

$$I_{Lr2_{\text{max}}} \cong 14.9 \text{ A}.$$

■ **Step 5**—Maximum value of the voltage across C_r ($V_{Cr_{\text{max}}}$).

From (19) and the parameters specified in Step 1, with (α) and (β), one can obtain

$$V_{Cr_{\text{max}}} \cong 695 \text{ V}.$$

■ **Step 6**—Nominal duty cycle of control (Dc_{nom}).

From Fig. 4, the duty cycle of control is given by

$$Dc = \frac{\Delta t_1}{T} + \frac{\Delta t_2}{T}. \quad (54)$$

From Fig. 6(b) and the parameters specified in the steps above, for nominal operation, we can obtain

$$q = \frac{V_o}{V_{\text{in}}} \cong 1.82, \quad \text{and} \quad Dc_{\text{nom}} \cong 0.291.$$

From (5) and (51), one can obtain

$$\frac{\Delta t_1}{T} \cong 0.03, \quad \text{and} \quad \frac{\Delta T}{T} \cong 0.13.$$

■ **Step 7**—The boost input inductance (L_f) and output filter capacitance (C_f).

With the parameters shown in the above steps, the boost inductance value L_f and the output filter capacitance value C_f to achieve the output ripple voltage less than 2% are specified as

$$L_f = 1.75 \text{ mH}, \quad \text{and} \quad C_f = 470 \mu\text{F}.$$

V. EXPERIMENTAL RESULTS

Fig. 7 shows the implemented circuit of the new ZCS-PWM boost converter.

Fig. 8(a) shows the voltage across C_r and the current through L_{r2} at full load. Fig. 8(b) shows the voltages and currents through diodes $D1$ and $D2$, also at full load. Fig.

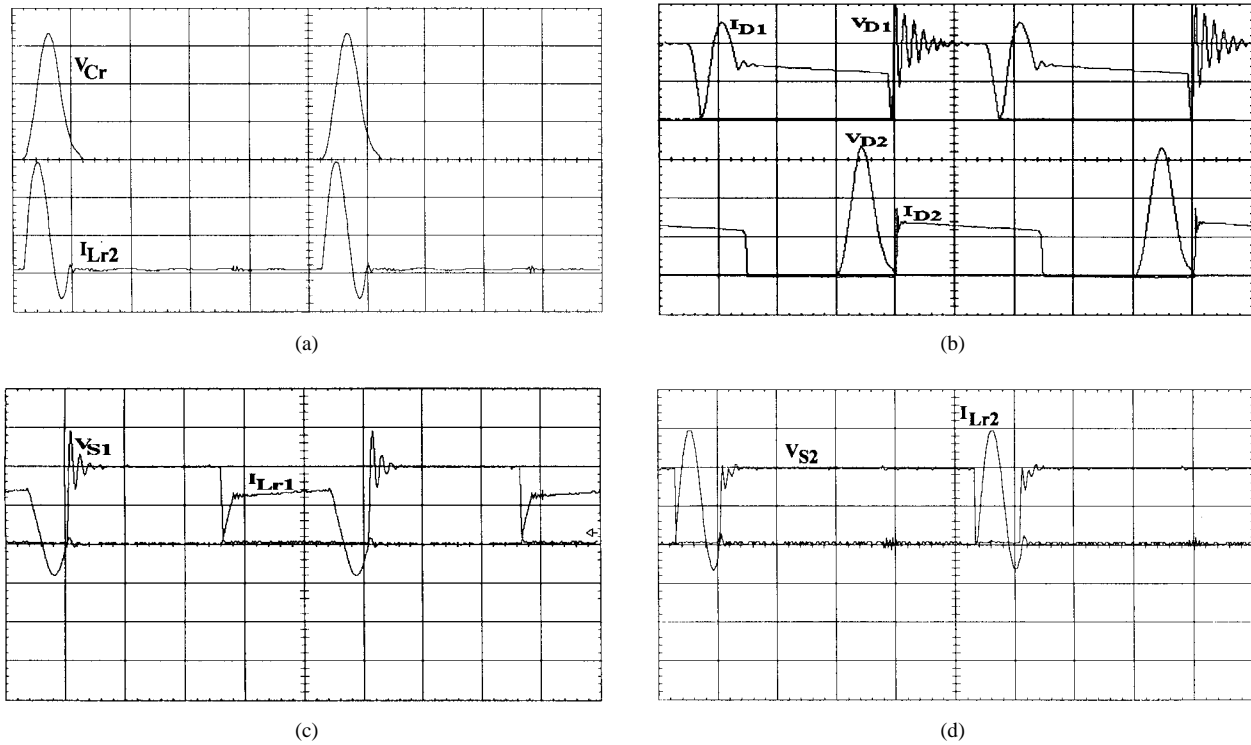


Fig. 8. (a) Voltage across C_r and current through L_{r2} . (b) Voltages and currents through $D1$ and $D2$. (c) Voltage across $S1$ and current through L_{r1} . (d) Voltage across $S2$ and current through L_{r2} at full load. Time scale: $10 \mu\text{s}/\text{div}$; voltage: $200 \text{ V}/\text{div}$; current: $5 \text{ A}/\text{div}$.

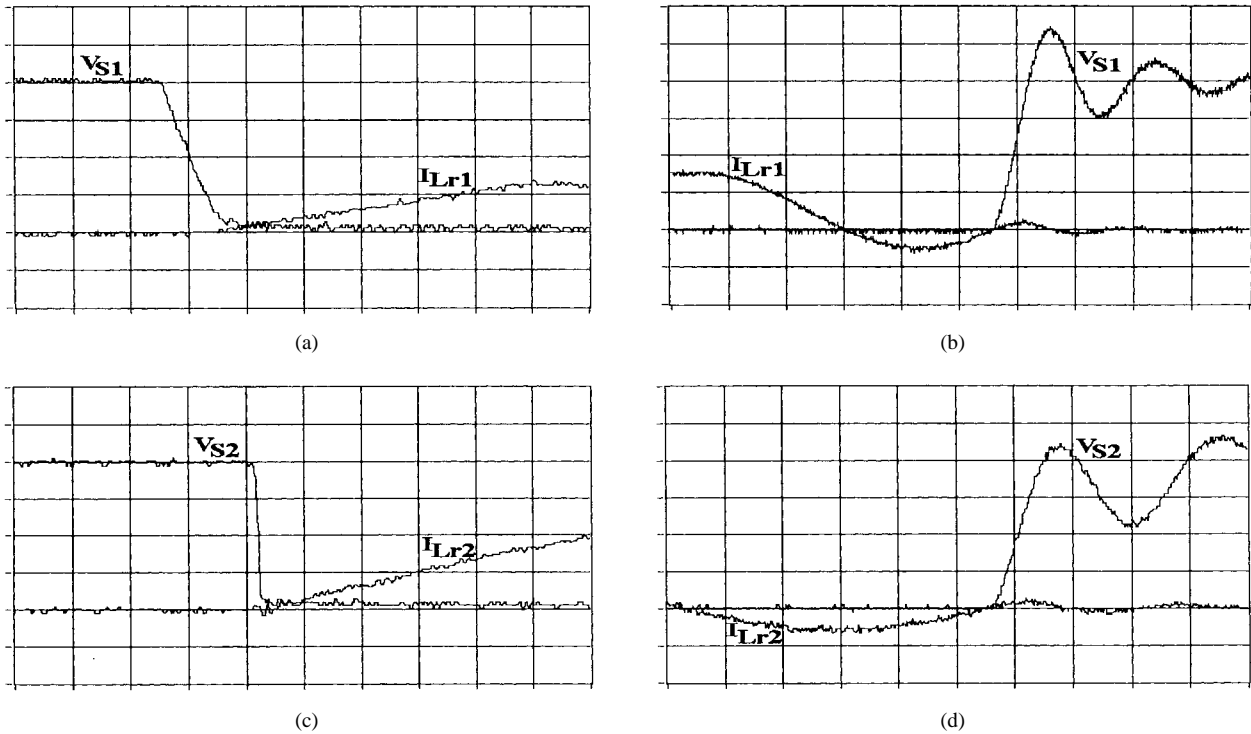


Fig. 9. Details of experimental waveforms for the new ZCS-PWM boost converter at full load. Voltage: $100 \text{ V}/\text{div}$; current: $5 \text{ A}/\text{div}$. (a) Time scale: $200 \text{ ns}/\text{div}$. (b) Time scale: $1 \mu\text{s}/\text{div}$. (c) Time scale: $200 \text{ ns}/\text{div}$. (d) Time scale: $400 \text{ ns}/\text{div}$.

8(c) shows the voltage across $S1$ and current through L_{r1} , at rated load. Fig. 8(d) shows the voltage across $S2$ and current through L_{r2} , also at rated load.

It can be seen that the results shown in Fig. 8(a) are in agreement with the theoretical analysis, and the maximum

values $I_{Lr2\text{max}}$ and $V_{Cr\text{max}}$ are determined by α and β . Furthermore, the results shown in Fig. 8(b) demonstrate that recovery problems do not exist, due to diodes $D1$ and $D2$.

Fig. 9(a) and (b) show the turn-on and turn-off instants, respectively, at the main switch ($S1$). Fig. 9(c) and (d) show

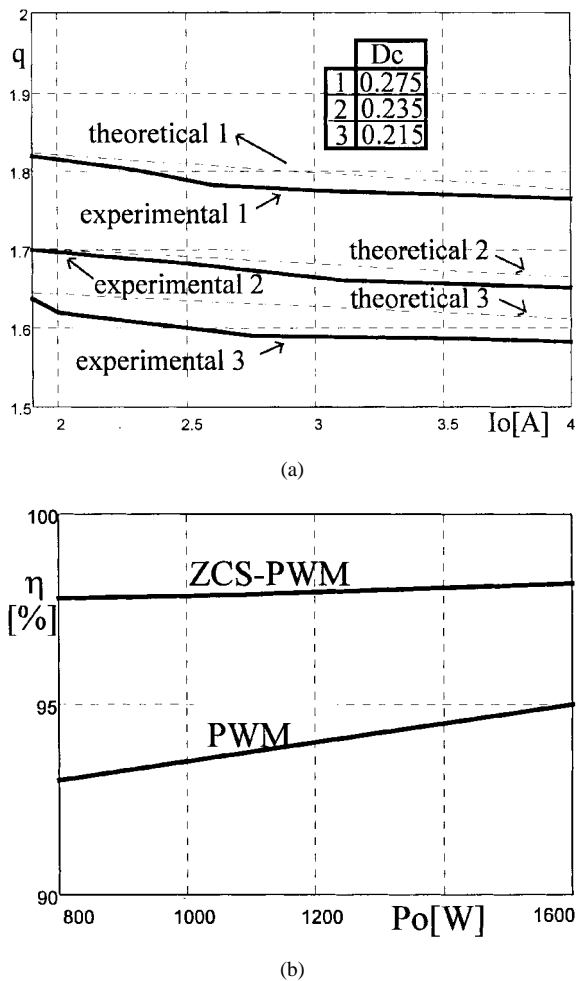


Fig. 10. (a) Experimental and theoretical output characteristics of the new ZCS-PWM boost converter. (b) Experimental efficiency comparison of the new ZCS-PWM boost converter and the conventional hard-switching PWM boost converter.

the turn-on and turn-off instants, respectively, at the auxiliary switch (S_2).

The experimental results, shown in Figs. 8(c) and (d) and 9, demonstrate that zero-current switching is achieved at constant frequency for both active switches (S_1 and S_2).

It should be noticed that diodes D_1 and D_2 were also softly commutated under zero-voltage switching [ZVS, Fig. 8(b)]. Therefore, the switching energy losses for this new ZCS-PWM boost converter are practically zero.

The experimental and theoretical dc-voltage conversion ratio characteristics of the new ZCS-PWM boost converter are shown in Fig. 10(a). These results are in agreement with the theoretical results from (43) and shown in Fig. 6(b). Fig. 10(b) shows the efficiency measurement of the new ZCS-PWM boost converter as a function of the output power, in comparison with the conventional hard-switching PWM boost converter's efficiency, at the same input and output data and operating at the same switching frequency (20 kHz).

The experimentally obtained efficiency from the new ZCS-PWM boost converter is equal to 98% and, from the conventional hard-switching boost converter it is equal to 95%, for rated load.

Therefore, the new ZCS-PWM technique significantly improves the circuit efficiency, and the average total power dissipation in the devices can be reduced by more than half, providing a great reduction in the size of the heatsinks used.

However, the price paid is the addition of a small auxiliary switch, two small resonant inductors, one small resonant capacitor, and one diode, in relation to the conventional PWM boost converter. It should be pointed out that this auxiliary resonant network only handles a small fraction (approximately 10%) of the total output power.

VI. CONCLUSION

This paper has presented a new family of ZCS-PWM converters. The operation of the proposed converters was analyzed using the new ZCS-PWM boost converter, employing IGBT's as the power switches, and rated at 1.6 kW.

Theoretical studies and experimental results of this new ZCS-PWM boost converter, taken as an example, allow us to draw the following conclusions.

- Soft commutation (ZCS) is achieved for the active switches, from nonload up to full load.
- The passive switches were also softly commutated (ZVS).
- The converters are regulated by the conventional PWM technique, at constant frequency.
- Latching of IGBT's due to turn-off never occurs; this relieves its reverse bias safe operating area (RBSOA) stresses.
- Low conduction losses are verified in the devices, in spite of an additional diode in series with the load.
- The average total power dissipation in the devices can be reduced by more than half, when compared with the hard-switching method, thus, providing a great reduction in the size of the heatsinks.

Therefore, the new ZCS-PWM boost converter combines the advantages of the PWM and ZCS techniques, without additional current and voltage stresses, in comparison with the conventional hard-switching method, improving the converter performance and maintaining high efficiency.

The new ZCS-PWM boost converter is appropriate for high-power and power-factor correction applications.

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